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The Front-End Electronics of the HADES timing RPCs wall: design, development and performances analysis

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CERTIFICA

Que a tese titulada "The Front-End Electronics of the HADES timing RPCs wall: design, development and performances analysis", foi realizada por D. Daniel Belver Fernández no Departamento de Física de Partículas de Universidade de Santiago de Compostela baixo a súa dirección, para acadar o título de Doutor en Física.

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Asinado:

Juan Antonio Garzón Heydt

"It's better to burn out
than to fade away..."

"Hey Hey, My My"
- Neil Young

Agradecementos

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Chapter 1

Introduction

Modern experiments in Particle and Nuclear Physics are characterized by their complexity. In order to resolve the very small scales that are typical in these fields, very huge and sophisticated equipments are necessary: high energy and high luminosity accelerators, big spectrometers, high resolution and high efficiency detectors together with several analog and digital electronic devices as well as fast and powerful computing equipments. Sometimes the support often requires setting up worldwide initiatives.

The central elements in such structure are the particle detectors. Presently, most detectors used in Particle Physics experiments belong to the family of electronic detectors. Particles going through them start some kind of ionization, excitation or pair-hole creation processes that induce electric pulses which are at the origin of the measurement of its properties: position, trajectory, time of flight, energy, velocity, etcetera.

The Front-End Electronics, FEE, is the first element of a detector to handle the electrically created pulse, and to drive it to the data acquisition system. Normally, its task is to preamplify the electric pulse, while keeping its main characteristics, before entering the amplifying and digitizing electronics. Sometimes, the digitization takes place at the FEE allowing for easy transport of many signals through twisted pair flat cables, several meters away from the detector down to the acquisition system. This is the case of the FEE developed for the new timing RPC wall that is being installed in the HADES experiment, at the GSI Helmholtzentrum in Darmstadt, Germany.

HADES (High Acceptance Di-lEpton Spectrometer) is a new generation spectrometer, designed for analyzing the properties of the vector mesons produced in heavy ion collisions in the range of 1-2 A.GeV. There are theoretical arguments predicting the modification of the properties of the matter at that energies as a consequence of the partial restoration of the Chiral Symmetry. Leptons are not affected by the strong interaction with the dense nuclear matter produced in the

collision, making the e^+e^- decay channels of the vector mesons the best the best place to test that predictions. As the dilepton decay chain is highly suppressed (depending on the vector meson, only one in around 10^4-10^6 decays follows that channel), a high acceptance and high resolution spectrometer of new generation was built at the GSI for that purpose. The HADES construction started in the middle of the nineties and, some years ago, an upgrade was approved in order to provide the spectrometer with a new high resolution timing detector for trigger and lepton identification purposes. This detector, based on the timing RPCs (Resistive Plate Chambers) technology, has been developed and built in the framework of a collaboration between the LabCAF of the USC, the LIP of Coimbra, the GSI and the IFIC of Valencia.

RPCs were chosen for the timing wall of HADES due to the competitive performances they offer at an affordable price to cover big surfaces. The development of RPCs was consolidated in 1981, when gaseous detectors under parallel geometries were operated at atmospheric pressure and at very high electric fields, providing a very fast narrow time response. This first RPC achieved very promising performances, reaching a 97% efficiency and a time resolution at the level of 1 ns, becoming a low price alternative to the plastic scintillators. In 2000, the importance of the mechanical uniformity of the gap in relation with high precision timing together with the development of fast amplification electronics, made it possible to operate a multi-gap RPC in avalanche mode with thin gaps of 0.3 mm (the timing RPCs or tRPCs), improving the time resolutions up to 50 ps. With time resolutions below 100 ps, the tRPCs found new applications in Nuclear and Particle Physics experiments in the field of particle identification (PID).

The readout preamplifying FEE plays a very important role for achieving the high time resolution that the tRPCs offer. The small gaps implemented in the timing RPCs, together with small charges of their signals, demand a high gain and bandwidth readout electronics in order to the best time resolutions. The fast signals produced in the detector are characterized by rise times at the level of $\sim$300 ps, requiring amplifying electronics with a bandwidth over 1 GHz.

The work presented in this memory describes the simulation, design, development, testing, manufacturing, installation and commissioning work of the FEE of the HADES tRPC wall. It covers all the steps starting from an obsolete but high performance 1-channel 2-boards design done at LIP Coimbra, up to a 4-channels, low consuming and compact design based on a motherboard-daughterboard philosophy. The amplifying and digitizing board provides both time and charge measurements codified in the LVDS output signal. The charge is measured through the 'Charge to Width' algorithm (QtoW). Almost 3000 channels have been built in order to instrument the six sectors (plus one spare) needed to cover the 8 m^2 of the small angle region of HADES.

The readout electronics was developed in collaboration with the CIEMAT of Madrid and the GSI of Darmstadt as a part of a more general project involving also the development at the GSI of the associated data acquisition board based on CERN's HPTDC circuits. FEE have been already installed and tested.

The main requirements the FEE of the HADES tRPC wall was asked to fulfill before undertaking the project were:

- A large bandwidth to deal with very narrow RPC pulses.
- Both precise timing and charge information in a single LVDS digital output signal through the 'Charge to Width' algorithm (QtoW).
- A multiplicity output to provide this information to the HADES trigger logic.
- Stability and a compact design for a moderate power consumption.

The HADES spectrometer and the design of its tRPC wall are presented in chapter 2 and chapter 3. The FEE is introduced in chapter 4 where first steps are also included. A simulation developed for the motherboard-daughterboard configuration can be found in chapter 5. Taking into account this simulation, chapter 6 is devoted to the improvement of the design and to the analysis of the performances of the board, together with a detailed analysis of the data of the first beam time test done at GSI during November 2005 using one of the final RPC prototypes.

Chapters 7 and 8 are devoted to explaining the last designs of the electronics and the analysis of their performances, respectively, together with other some small tests. The results of a detailed analysis of a beam time test done at GSI in October 2007 with a full equipped RPC sector, with 1116 cells and 2232 FEE channels, placed at its nominal position in the HADES spectrometer, are presented in chapter 7. The commissioning of the whole project and the final installation are included in chapter 8.

The final chapter is devoted to the conclusions and a summary of the work done to achieve the final design and the performances reached. Some technical details of the readout electronics, including the schematics and layouts of the different FEE steps, are included in the Appendix sections.

Chapter 2

The HADES experiment

2.1 Introduction

The investigation of nuclear at high temperature and high density is one of the major research topics in modern Nuclear Physics. Nucleus-nucleus collisions at relativistic energies offer the unique possibility to create such highly excited nuclear matter in the laboratory [1], [2]. These investigations are essential to understand processes like the birth of the Universe in the Big Bang and its later evolution. This line of investigation contributes also to obtain the equation of state of nuclear matter which is not only important in Nuclear Physics, but also to understand physical processes taking place during the latest stages of stars evolution.

The work presented here has been done in the framework of the international HADES[1] Collaboration, composed of 19 institutions from 9 European countries and with almost two hundred scientists. The High Acceptance Di-Electron Spectrometer (HADES) is the name of the full detector system, consisting on several instruments working together in one spectrometer, and it is placed at the GSI[2] institute in Darmstadt, Germany, together with the required particle accelerator. HADES is focused to study of in medium modifications to the properties of the vector mesons. Calculations based on QCD (Quantum Chromo Dynamics) and some hadronic models, predict detectable changes in the width and mass of hadrons produced in dense nuclear medium. From the point of view of QCD such modifications could be a signal of the so called *chiral symmetry restoration*. The main goal of HADES is to provide experimental insight for the study of QCD on the non disturbed regime and possibly see a signal of the expected chiral symmetry restoration.

A new timing RPC[3] detector wall was proposed for HADES by LabCAF-USC and LIP-Coimbra to improve the ToF and high level trigger performances at small angles. It is presented in Chapter 3, together with its physics. The electronics developed for this RPC wall and some results are presented along this work.

[1] High Acceptance Di-Electron Spectrometer.
[2] GSI Helmholtzzentrum für SchwerIonenforschung GmbH.
[3] Resistive Plate Chambers.

2.2 The HADES physics

HADES is a unique apparatus assembled at the heavy ion synchrotron SIS at GSI Darmstadt. The main part of the HADES physics program is focused on studies of in-medium properties of the light vector mesons ρ (770 MeV/c^2), ω (783 MeV/c^2) and ϕ (1020 MeV/c^2) [3], [4]. The spectrometer is also able to detect and study the properties of hadrons and this is an important task.

Significant changes of the vector meson spectral functions in hot and/or dense nuclear matter have been predicted by various models. The meson spectral functions inside nuclear matter are directly accessible via a measurement of the dielectron invariant mass distributions of the two-body meson decays because e^+e^- pairs do not suffer from a strong electron-hadron final state interaction. A low mass dielectron excess observed in heavy ion collisions by the CERES experiment on SPS at CERN [5] launched an exciting dispute about its origin. According to QCD inspired models, this excess can be considered as a signal of the partial *chiral symmetry restoration* in dense and hot nuclear matter. On the other hand, various hadronic models explains this enhancement by significant in-medium modifications of the ρ meson spectral function due to strong meson couplings to low lying nucleon resonances [6].

At SIS, energy domain dielectron invariant mass distributions were measured in proton-proton and light and heavy ion reactions by the DLS collaboration at the BEVALAC [7], [8]. Within the given experimental errors bar, the extracted e^+e^- production rate in p-p reactions could be reasonable reproduced by theoretical calculations assuming free dielectron decays of various hadronic sources [9]. For the heavy collisions Ca+Ca and C+C, a remarkable excess of the dielectron yield in the low mass range 200 MeV/c^2<M_{inv}<600 MeV/c^2 as compared to the theoretical calculations was found. This dielectron excess could not be explained neither by hadronic models based on the in-medium modified ρ meson spectral functions nor by the Brown-Rho scaling [10].

In order to study the high density phase, light vector mesons are a well suited probe. Their lifetimes (see Table 2.1) are short enough for them to have a significant chance of decaying in the same dense medium where they were created. When they decay, they may do so in two leptons. Since leptons do not experiment strong interaction, when they leave the interactions zone they retain memory about how they were produced. Hence they carry information about the properties of the mesons in the dense medium. If their masses or widths have changed due to a partial restoration of chiral symmetry we should be able to observe it by looking at the lepton pairs' invariant masses. Predominant dilepton sources for m(e^+e^-)>600 MeV/c^2 are direct or Dalitz decays of the light mesons ρ, ω and ϕ produced in these collisions.

The main problem is the low branching ratio for the dilepton channel in the vector meson decays. This needs to be compensated with high statistics and a powerful trigger scheme, which translates into a need of a high acceptance spectrometer and high beam intensities. Another problem is the presence of several background

Meson	Mass ($\frac{MeV}{c^2}$)	Width ($\frac{MeV}{c^2}$)	$c\tau$ (fm)	Dominant channel	e^+e^- branching ratio
ρ	775.8	150	1.3	$\pi\pi$	4.67×10^{-5}
ω	782.6	8.49	23.4	$\pi^+\pi^-\pi^0$	7.14×10^{-5}
ϕ	1019.5	4.26	44.4	K^+K^-	2.98×10^{-4}

Table 2.1: *Life vector mesons life times [11].*

sources, like pion Dalitz decays, which also produce leptons and lepton pairs, so that the vector meson signal is sitting on a continuous background.

Vector mesons are hadrons composed by a quark and an anti-quark. ρ, ω and ϕ mesons have different properties concerning lifetimes, widths or lepton pair branching ratios. It seems that ρ meson is the more suitable to be used as a probe since it has a large chance of decaying in the dense zone but, nevertheless, all of them contribute and will be studied.

The HADES experiment [4], described below, aims at systematic studies of dielectron production in proton, pion and heavy ion induced reactions. Although beam energies available at the GSI/SIS facility are limited to the kinematic region near the vector meson production threshold, this domain is interesting for confirming the unexplained DLS results as well as for the understanding of vector-meson hadronic couplings involved in the interpretation of the CERES data. The experiment will allow us for the first time to measure several elementary dielectron production channels in nucleon-nucleon and pion-nucleon reactions using exclusive measurements.

2.3 The HADES spectrometer

In order to provide an answer to the 'DLS puzzle' and to further study in medium effects up to Au+Au collisions at E_{kin}=1.5 GeV/A, the High Acceptance Di-Electron Spectrometer HADES was conceived and built at GSI, Darmstadt, Germany [3], [4]. Therefore, it is a second generation experiment in dilepton spectroscopy that aims at measuring the invariant mass of the light pseudovector mesons in heavy ion collisions. That goal puts a number of requirements on the design of HADES.

The design of HADES is governed by the high-multiplicity environment of heavy ion collisions, the production cross sections below threshold and the small branching ratio for the dilepton decay channel due to the electromagnetic coupling constant. Only one of 10^5-10^6 central Au+Au collisions will produce an e^+e^- pair from a meson decay. For this reason, the main features of the new instrument are:

- Large acceptance and sufficient granularity in order to maximize the probability to detect a pair once it is produced. The geometrical acceptance of $\sim$40% [3] represents an improvement by a factor of 100 as compared to the pioneering experiments performed with the DLS spectrometer at Berkeley.

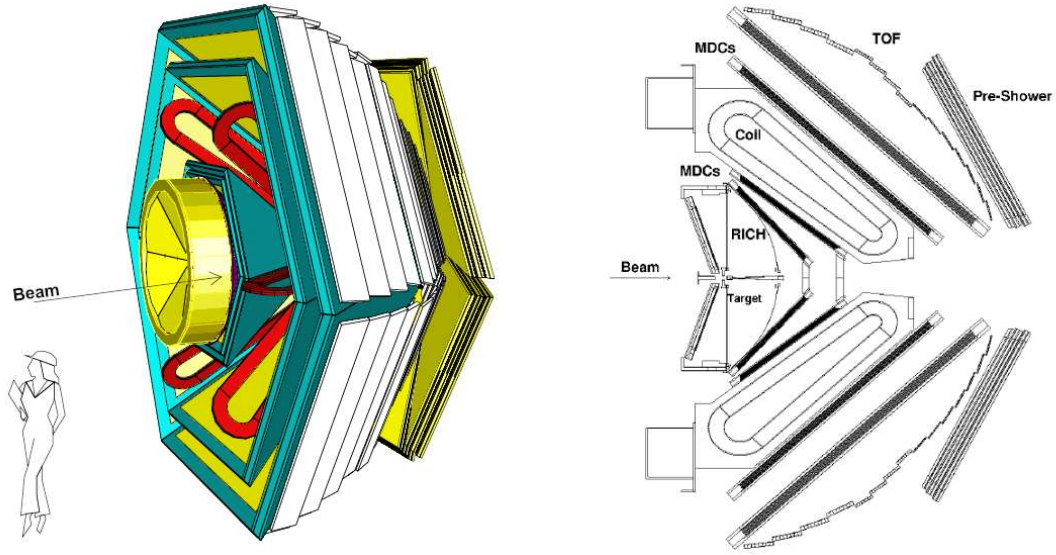


Figure 2.1: *Left: 3D view of the HADES spectrometer, showing its hexagonal symmetry. Right: azimuthal cross section of HADES, indicating its detectors.*

- High count rates need to be supported. The goal is to be able to operate with beam intensities as high 2×10^7 particles per second.
- A trigger system able to downscale the amount of raw data by several orders of magnitude. This trigger scheme in HADES is made of two stages, ideally the joint rejection power would be in the order of 10^4.
- A high resolution for invariant mass reconstruction, in the order of the ω width in the mass region of the ω, being $\frac{\Delta M_{inv}}{M_{inv}}$=1% and a signal to background ratio larger than one for invariant masses up to $M\simeq$1 MeV/c^2.

Figure 2.1 shows an schematic view of the HADES spectrometer, where its characteristic hexagonal symmetry (left side) and its constituting detectors (right side) can be appreciated. It shows how it is divided azimuthally in six identical sectors, each covering polar angles between 18°<θ<85°, with practically full azimuthal coverage, besides the shadow regions introduced by the coils and detector frames. This gives an acceptance for lepton pairs of 40%.

HADES is part of the accelerator system placed at GSI, which consists in a linear accelerator (UNILAC) injecting ions into a 60 m diameter synchrotron (SIS18), from where the beam can be extracted to the Fragment Separator (FRS), to the Electron Storage Rings (ESR) or to the experimental areas. Figure 2.2 shows a picture of the whole GSI accelerator area.

The UNILAC was built in 1975 and upgraded in 1999 thanks to the development of a new high current injector, called HSI. It provides an increase in the beam intensity that is able to fill the synchrotron up to almost its *space charge limit* for

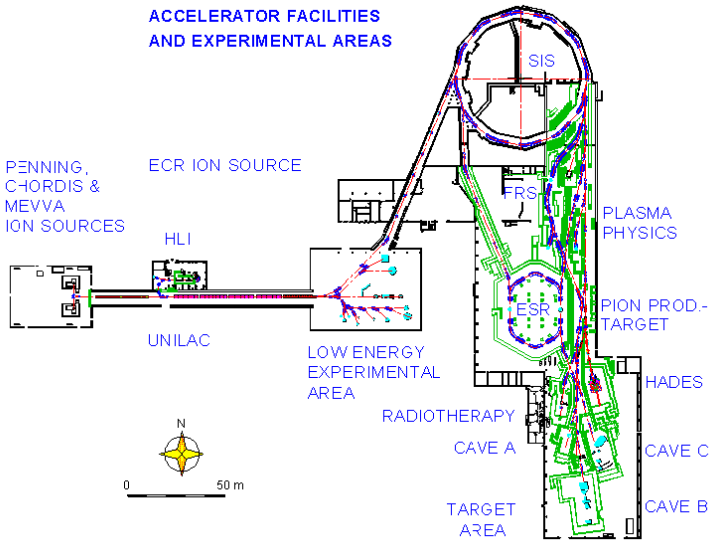


Figure 2.2: *GSI's accelerator.*

all ions ($I \simeq 10^{11}$ ions for C beam and $I \simeq 10^{9}$ ions for Au beam). After stripping and charge state separation, the beam from the HSI is matched to the UNILAC, which accelerates the nuclei up to a few MeV/A, feeding the SIS. The SIS is a synchrotron with a circumference of 216 m, consisting in 24 bending magnets and 36 magnetic lenses to focalize the beam until each experiment.

The SIS18 is being upgraded towards the so-called SIS200 within the future project FAIR[4]. It will be able to ultimately reach intensities as large as $I \simeq 10^{12}$ ions/spill for heavy ions and energies up to 30 GeV/A [12].

The story of an ion collision in HADES is as follows:

1. An ion beam comes from the SIS accelerator at typical energies $E_{kin} \simeq 1$ GeV/A and is deviated to HADES cave (coming from the left on Fig. 2.1).

2. Before and after interacting with the target, a coincidence/anti-coincidence system (START/VETO) provides a signal corresponding to an interaction.

3. The outgoing sub-products cross a threshold RICH blind to hadrons.

4. Next, a very high precision MDC system tracks the particle before the toroidal coils of the magnet. After the magnet, two more MDCs track the particle for a good measurement of the bending after the magnet.

5. A TOF wall is devised for lepton identification after the magnetic field.

6. At low polar angles a SHOWER detector improves the rejection capability of last pions.

[4]Facility for Anti-proton and Ion Research.

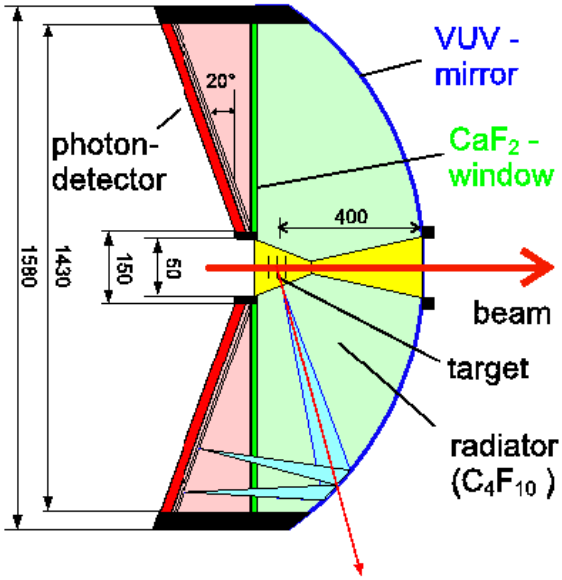


Figure 2.3: *Side view of the RICH detector.*

Next, we will present in detail the different detector systems of the HADES spectrometer from inner to outer.

2.3.1 The START and VETO detectors

Both detectors, placed 75 cm before (START) and after (VETO) the target, consist on two identical fast diamond detectors. The system is aimed at working such that a valid signal on START and null on VETO results in a valid start signal, that must be delivered faster than 1 MHz. The detector-electronics yields a time resolution up to 29 ps being rate resistant beyond 10^8 ions/s per channel for meeting the HADES requirements [13]. The detector is conceived to provide a VETO efficiency ε>96.5%, over an area A=2.5 cm×1.5 cm (matching the beam spot).

A new START detector system is needed for high intensity proton beams. It consists on 96 channels of scintillating fibers of 1 mm diameter, featuring high efficiency up to rates of 10^8/s, a time resolution below 500 ps and a high granularity [14]. Two prototypes of 16 channels each and one fully equipped detector were used, respectively, in the HADES proton commissioning beam time in 2003 and in 2004.

2.3.2 The RICH detector

The Ring Imaging CHerenkov (RICH) [15] is the first detector found by the products of the primary interaction. It consists of a gaseous radiator surrounding the target in the forward hemisphere, a spherical mirror and a position sensitive UV detector (see Fig. 2.3). It is a crucial detector for lepton identification, being totally blind to hadrons while providing a very low multiple scattering and γ conversion

probability, due to its gaseous low Z radiator, namely, C_4F_{10}. The low refraction index of the radiator gas provides a threshold for Cherenkov emission γ_{th}=18.2, sensitive to electrons with momenta above 10 MeV. On the other hand, it is blind to pions up to energies of around $E_{kin}\simeq$2.5 GeV, which is by far above the maximum kinetic energies available at SIS.

The Cherenkov radiation is very softly attenuated by absorption within an UV window corresponding to 145 nm$<\lambda<$190 nm. The Cherenkov light emitted in a cone is reflected by a spherical carbon fiber mirror (2 mm thick) to the back part of the system where they are detected, being focused as a ring image on a position sensitive UV photon detector plane.

2.3.3 The MDCs and the magnet

The Multi-wire Drift Chambers (MDCs) [13] are in total 2×2×6 chambers, namely, 6 sectors with two groups of two MDCs before and after the magnet (I/II and III/IV, respectively). MDCs were designed to provide track reconstruction before and after the magnetic field with position resolution $\delta y\leq$100 μm (σ). This extremely high position resolution allows to obtain a momentum resolution $\Delta p/p\simeq$1% and therefore $\Delta M/M\simeq$1% for the invariant mass, fulfilling the requirements of the HADES technical proposal [16].

The MDC chambers consist of six-wire planes at different angles, with cells sizes ranging from 5×5 mm^2 (inner plane) to 14×10 mm^2 (outer plane) and filled with a He/iso-C_4H_{10}. The total thickness of the four MDCs chambers amounts to x/X_0=0.2% only, comparable to the contribution of the air volume between the target and the outer MDC IV.

In between both groups of MDCs (see Fig. 2.1), a superconducting magnet consisting of six coils, produces an inhomogeneous magnetic field which reaches a maximum value of $B\simeq$3 T near the coils, down to $B\simeq$1.5 T in the acceptance region. The track momentum is reconstructed from the deflection in this magnetic field.

2.3.4 The TOF wall

TOF and TOFino[5] [17] are time of flight detectors aimed at providing a high timing resolution for separation of leptons from fast pions. Both are required for implementing the multiplicity condition to select different centralities of the primary collisions, the so-called first level trigger. Redundant identification of the electron tracks is achieved via time of flight measurement. A 3D picture of the TOF wall system is shown in Fig. 2.4.

The TOF detector is made of plastic scintillator rods (BC408) read at both ends by EMI 9133B photo-multipliers. Therefore, an unbiased estimate of the time of

[5]TOFino is being replaced by the tRPC wall we are developing, being the development of the FEE of the RPC the main topic of this work.

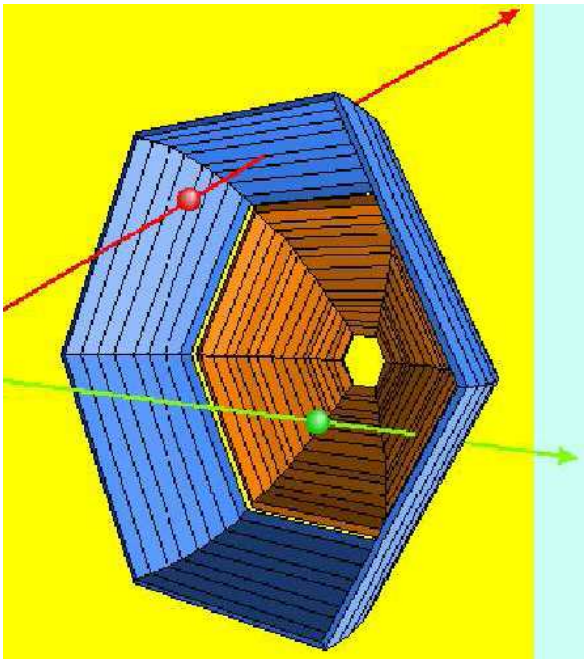


Figure 2.4: *3D view of TOF (at high polar angle region) and TOFino (low polar angles) detectors.*

flight and impact position can be obtained, yielding $\sigma_T \simeq$100-150 ps and $\sigma_x \simeq$1.5-2.3 cm. The pad profile is a 2.0×2.0 cm^2 rectangle for the inner four sets and 3.0×3.0 cm^2 for those at larger polar angle. They are grouped in sets of eight, with eight such sets per sector, covering the laboratory large polar angles $45° < \theta_{lab} < 85°$.

At polar angles below 45°, the TOFino time of flight detector is temporary placed in order to fulfill the minimum requirements that allow to explore the low multiplicity reactions, providing a reasonable multiplicity trigger still. TOFino consists on four scintillators with single read-out (see Fig. 2.5) and time resolution $\sigma_T \simeq$350 ps after correcting for the position of the interaction.

As was previously explained, in order to cope with the high multiplicities present in typical Au+Au collisions at 1.5 GeV/A, the TOFino is being replaced by a timing RPC wall with a granularity 80 times larger and time resolutions well below 100 ps.

2.3.5 The SHOWER detector

According to [17], fast pions will emulate di-leptons (*fake*) by an amount of 2-3 per event in Au+Au collisions at E_{kin}=1 GeV/A, for a time resolution os σ_T=100 ps. The effect is reduced for the large polar angle region, where less than 1 fake per event is expected. Because of this fact, it was decided to place an electromagnetic shower detector behind the TOFino wall, in order to increase hadron rejection.

Figure 2.5 shows a picture of the SHOWER detector layout, together with the TOFino. Each sector of the SHOWER is constituted by three sensitive planes of

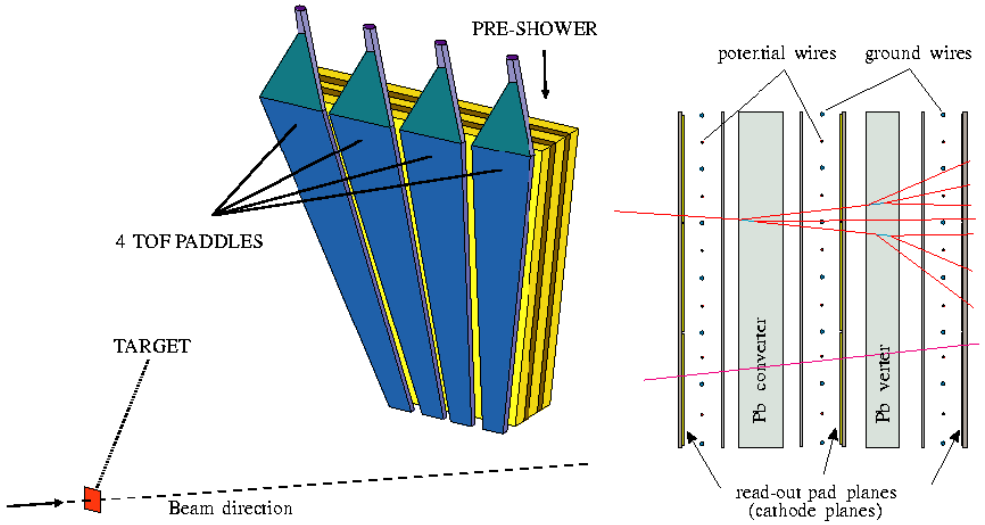


Figure 2.5: *The SHOWER detector and the TOFino [18], [22].*

wire chambers with signal pick-up in pads of squared shapes, ranging in heights from 3 to 4.5 cm. The sizes ensure an occupancy below 5% for Au+Au collisions [18]. Between the active layers, two lead converters are interposed, aiming at inducing an electromagnetic shower with a high probability, but still keeping the probability of hadronic shower at low levels.

The interposition of lead converters defines in a naturally way the so-called Pre-Shower, Post-Shower1 and Post-Shower2 sub-detectors. Chambers are operated in Self Quenching Streamer mode. A 'shower condition' can be defined through the ratio of the charge collected in each of the two Post-Shower detectors to the one collected in the Pre-Shower, allowing to identify leptons.

2.3.6 The trigger scheme

In order to enhance the 'interesting' events and reduce the collected data to a manageable set, the data acquisition is based on two trigger levels:

1. The positive first level trigger (LVL1) is given by a fast t_f<100 ns hardware analysis of the multiplicity measurement M_{ch} performed by the TOF modules. It is expected from simulation that, in Au+Au collisions, this multiplicity condition leads to a selection of 10% of the total number of collisions.

2. The second level trigger (LVL2) performs a three-steps process:

   In the first step a search for electron ring images on the RICH pad plane is made. In parallel, charge clusters with the signature of an electromagnetic shower in the Pre-Shower detector as well as particles with an appropriate time of flight in the scintillator TOF wall are searched for.

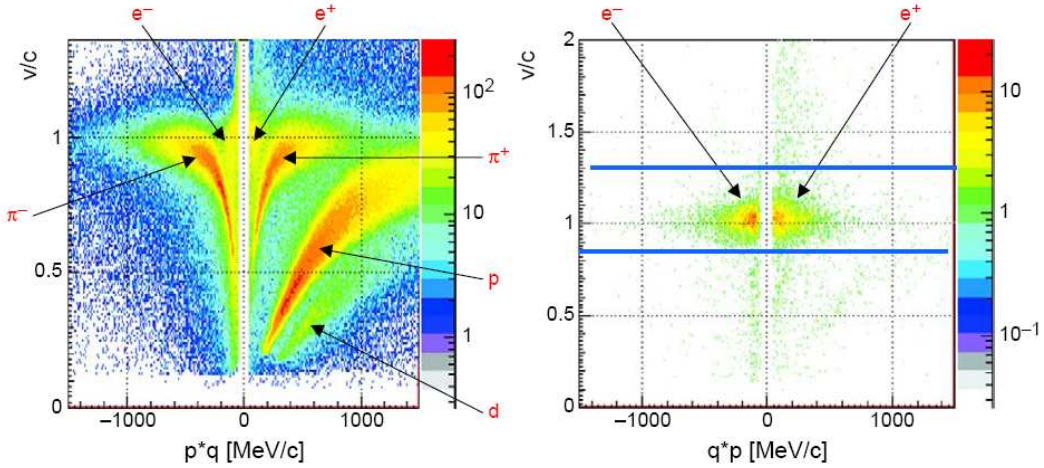


Figure 2.6: *Left: β vs p distribution for all reconstructed particles (LVL1) from C+C at 2 GeV/A. Pions and proton branches are clearly resolved. Right: the same plot after imposing all the cuts for rejecting hadrons. The last cut, namely a cut in the time of flight of the particles, is graphically shown. The intensity scale is logarithmic.*

The resulting position coordinates of electron candidates in the inner RICH and outer TOF detectors are compared in the Matching Unit (MU) in an appropriate matching window, taking into account the track deflection due to the magnetic field. The matched hits define a valid electron candidate track.

In the third step, the selected electron tracks with opposite charges can be combined into dielectron pairs and their invariant mass can be calculated on the basis of a look-up table which contains a mapping of the polar electron track deflection angles to momenta.

In order to avoid losing too many events after applying both level triggers, the LVL2 trigger must be generated in less than 10 μs, allowing for a reduction in the candidate tracks up to a factor 100, and yielding a data flow of 1 KHz. Results in a 2 GeV/A C+C collisions imposing a conservative LVL2 trigger condition requiring at least one electron track, indicate a reduction of a factor 12, providing 92% background event rejection and high electron identification efficiency (ε>70%).

An example of this procedure, taken from [4], is shown in Fig. 2.6. The shapes of the momentum spectra for electrons and positrons are very similar to each other, measured with C+C collisions at 2 GeV/A. The extreme capability of hadron rejection is apparent, being the average multiplicity of the lepton tracks as low as 2×10^{-2} per LVL1 event.

Chapter 3

Timing RPC detectors: the HADES tRPC wall

3.1 Historical RPC introduction

3.1.1 RPCs

RPC, the acronym for Resistive Plate Chambers detectors, are playing an important role nowadays not only like counter detectors but also like timing detectors (tRPCs). The origin of the RPCs is the Parallel Plate Chamber (PPC), which consists in two parallel metallic electrodes operated at high voltage, thus providing an uniform electric field across its volume. A charged particle crossing the space between electrodes creates electron-ion pairs. If the field is high enough, the released electrons are accelerated towards the anode, regaining enough energy for inducing further ionizations in a cascading process called avalanche (*gas multiplication* [19]), producing a measurable charge from a reduced number of initial charges.

The operation of parallel geometries with electrodes covered by high resistivity materials was pioneered in 1971 [20]. The Pestov's group used a highly resistive material (glass) for limiting the progress of the spark created, working in quenched spark mode. The so-called 'Pestov counter' [20] was able to achieve ultimately a time resolution of 25 ps, although it was characterized by its high technical complexity.

This technology was consolidated in 1981 with the appearance of the Resistive Plate Chambers (RPCs) [21] developed by R. Santonico and R. Cardarelli. The idea was overcame the difficulties of the Pestov counter [20], keeping its more fundamental virtues. This first RPC [21] consisted in two parallel copper electrodes covered with high resistance plates made of a phenolic resin known as Bakelite, with a volume resistivity $\rho \simeq 10^{10}$ Ωcm. The ensemble delimited a single gap of 1.5 mm filled with a gas mixture of $Ar/iso - C_4H_{10}$ (iso-butane is an UV quencher, while Argon is a noble gas well suited for gaseous detectors due to its high density) in a proportion 1:1 (see single-gap RPC design on Fig. 3.1). The very fast drifting electrons produce a signal with large charge (100 pC) that can be used for timing purposes, whereas the

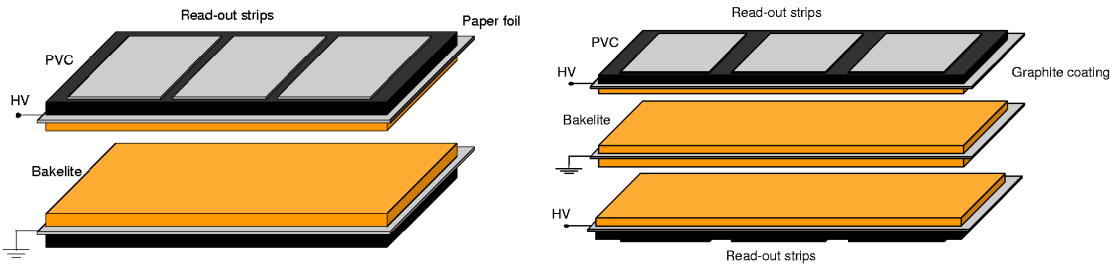


Figure 3.1: *Examples of a single gap RPC [21] (left) and a double gap RPC [23] (right), according to their original designs. Dimensions are not realistic, in particular, the gap has been enlarged (pictures from [22]).*

ions drift to the cathode at much smaller velocities, due to their higher mass. The signal was measured with pick-up strips, separated from the High Voltage through PVC[1], avoiding the use of coupling capacitors. The HV has to be applied through a non-perfect conductor in order to be transparent to the induced signal (Fig. 3.1-left).

Under these conditions, the dark rate of the counter was considerable, contributing to a decrease in the efficiency. For avoiding this effect, the plates were painted with linseed oil and this technique has been kept since then for Bakelite-based RPCs. The main advantage as compared to the Pestov counter is that the gas circulates at atmospheric pressure. The large resistivity of the electrodes limits the current avoiding the progress of damaging processes like sparks or permanent discharges. But the high resistance of the electrodes also represents one of the main limitations of these detectors. Once the signal is produced, the area where the streamer develops is blind during a given transit time (∼ms for bakelite electrodes), and during this time the effective field in this region will be lower. As a consequence, if the counting rate is very high, one can expect fluctuations in the local field caused by earlier avalanches, reducing the efficiency and the time resolution.

The basic operation principle of an RPC is already described in [21] and not much has changed since then. The parallel geometry allows to extend the 'multiplication region' to all the detector (the field is high enough for inducing an avalanche at any point), while in proportional detectors it is required a propagation time along the 'drift region' before the multiplication can take place, affecting the timing properties.

The RPC technology achieved very promising performances with this first design, reaching a 97% efficiency and a time distribution of 1.2 ns FWHM, becoming an affordable alternative to the use of plastic scintillators, mainly in big surfaces.

3.1.2 Double gap RPC

Some years later, in 1988, the double gap structure in the RPCs was introduced [23] and the gap increased up to 2 mm, which is the common value nowadays. The setup was symmetric with the ground electrode in the center and the HV applied over

[1]Polyvinyl chloride.

the outer layers (Fig. 3.1-right). This 2-gap configuration allowed for an increase in efficiency and confirmed that the time resolution was well at the level of $\sigma_T \simeq 1$ ns.

3.1.3 Operation modes

Streamer mode

A streamer is a process of a different nature than avalanche multiplication (see section 3.1.1), releasing a high amount of charge as compared to a normal avalanche (therefore, it limits the rate capability that become a potential problem for RPCs operated in this mode). It requires high operation voltage. The secondary ionizations are so large that the charge created distorts the electric field, causing eventually a streamer in the detector gas. This mode has the advantage of providing larger signals that can be discriminated without amplification, simplifying the readout electronics as compared to the avalanche mode. RPCs in streamer mode are well suited for experiments that work at low rates (BaBar at SLAC [24] that operates $\sim$1 Hz/cm^2) and also for cosmic rays experiments as ARGO at YangBaJing [25].

This mode was also called 'spark mode' [26] but it is probably not a good choice and the term 'streamer mode' became more popular [27].

Avalanche mode

The avalanche mode was introduced in 1993 [28] as an attempt to improve the rate capability by reducing the charge released per avalanche (0.2 pC). It was also called 'proportional mode' [27], but this was a bit ambitious and the term 'avalanche mode' prevailed [26]. Gas mixtures with lower amplification are used in this mode, requiring a high-gain fast amplifiers integrated in the Front-End Electronics (FEE) to compensate this effect, being the FEE more complex than in the streamer mode.

RPCs operating in avalanche mode have found application in high energy physics (ATLAS [29] or CMS [30] at LHC) and are often called 'trigger RPCs', allowing for rate capabilities in the range 100-1000 Hz/cm^2. This RPCs have also found applications in timing detectors (like ALICE [31] at LHC or FOPI at GSI [32]).

3.1.4 Multi-gap RPCs (MRPCs)

In 1996, a new design appeared [33] developed by M.C.S. Williams' group, consists in a triple set of equally-spaced Bakelite plates separated by gaps of 3 mm, that divide the gas volume into individual gaps (see Fig. 3.2). HV can be applied to external surfaces and internal plates get a voltage which is the voltage applied to the external ones. This configuration allowed for a similar time resolution as a single gap 2 mm chamber reducing the dark current and increasing the efficiency.

It can be roughly expected that the multi-gap increases the efficiency as:

$$\varepsilon = 1 - (1 - \varepsilon_N)^N \tag{3.1}$$

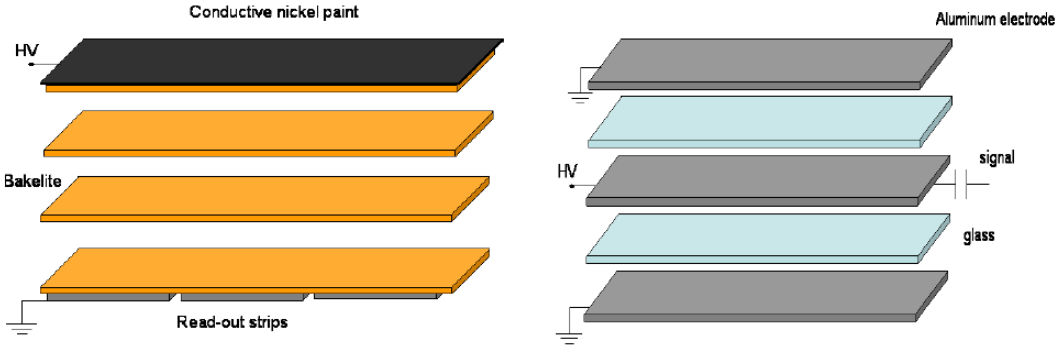


Figure 3.2: *Examples of two multi-gap RPCs [22]: the original 3-gap design [33] (left) and the 4-gap timing RPC prototype studied in the next chapters (right).*

where N denotes the number of gaps and ε_N the efficiency per single gap. Equation 3.1 is exact under the assumption that, for detection, at least one of the gaps must provide a detectable signal with independence of the others. But this assumption is not true, as two independent induced signals falling below the detection threshold can yield a total signal that is above it; therefore the efficiency represented by Eq. 3.1 represents a lower bound to the one expected in reality [22]. On the other hand, the time resolution slightly increases, in a first approach, as:

$$\sigma_T = \frac{\sigma_{T,N}}{\sqrt{N}} \tag{3.2}$$

which is the expected if the fluctuations in time response have a Gaussian origin [22]. It has been observed that σ_T depends on the gap width, typically improving for small gaps [34]. Then, a multi-gap design can provide a good timing, as characteristic of narrow RPCs, keeping the efficiency at high levels, typical of wide RPCs.

3.1.5 Timing RPCs (tRPCs)

The realization of the importance of the mechanical uniformity of the gap in relations with high precision timing together the development of fast amplification electronics, made possible to operate a multi-gap RPC in avalanche mode with thin gaps of 0.3 mm and glass electrodes, at fields as high as 100 kV/cm. This was done by P. Fonte, A. Smirnitski and M.C.S. Williams [35] in 2000. A new branch in the field was open, achieving a time resolution at the level of 120 ps, although the possibility to go down to the level of 50 ps for small detectors was soon confirmed [36]. The use of large size tRPCs was later confirmed [37], providing resolutions well below 100 ps, with reasonable homogeneity.

Soon after the first development, it became popular the use of standard window glass in RPCs, also called soda-lime-silica glass or just float glass [37]. It is widely available, affordable and still with a resistivity $\rho \simeq 10^{12-13}$ Ωcm, allowing for operation rates up to around 500 Hz/cm^2.

3.1.6 Gas mixture and operation voltage

Modern RPCs working in avalanche mode use mostly mixtures of tetrafluorethane ($C_2H_2F_4$) with 2% to 5% of isobutane (iso-C_4H_{10}) and 0.4% to 10% of sulphur hexafluoride (SF_6). iso-C_4H_{10} is an UV quencher which prevents from the appearance of secondary avalanches from gas photoionization. The addition of SF_6 extends the streamer free operation region, producing a shift in the efficiency plateau to higher voltages and an improvement in the stability and the time resolution [34].

Most of the timing RPCs used nowadays work with the so-called 'standard mixture' [38], based on the gas mixture explained above and where the proportions are $C_2H_2F_4$ (85%), SF_6 (10%) and iso-C_4H_{10} (5%), or slight deviations around it [22].

One of the factors which mainly determines the RPC performances is the electric field applied. Timing RPCs usually work at $E\sim$100 kV/cm [22], [35]. The efficiency of a tRPC is higher with high voltages. The problem is that the higher the field, the higher the probability of streamers. The working point has to reach a compromise between high efficiency, good time resolution and low probability of streamers.

3.1.7 Readout electronics

Readout preamplifying electronics (or Front-End Electronics) plays a very important role in the time resolution that can be achieved. This is due to the fact that the intrinsic time resolution of an RPC detector is very good ($\sigma\sim$50 ps [34]), therefore the total time resolution will be a quadratic sum of the intrinsic and electronics resolution. Different electronics chains have been developed in order to reduce this contribution to the total time resolution (see for example [78], [39]). Section 3.2.6. shows different readout electronics developed for timing RPC walls.

A compact and low-noise amplifying and digitizing FEE for the HADES tRPC wall has been developed, and will be more thoroughly described in the next chapters.

3.2 Timing RPC physics

As timing RPCs is the design used in our HADES RPC wall, its description will be developed in more detail in this section. However, most of the characteristics mentioned in the following can be extrapolated to standard RPCs.

3.2.1 Efficiency and primary ionization

The efficiency of an RPC is related to the average number of ionization clusters produced per unit length $n_0/g{=}1/\lambda$, being n_0 the average number of clusters, g the gap width and λ the mean free path for ionization of the primary particle. In the ideal limit where any cluster is detected, the intrinsic efficiency of the RPC is [22]:

$$\varepsilon_{int} = 1 - e^{-g/\lambda} = 1 - e^{-n_0} \tag{3.3}$$

and, by analogy, the efficiency measured in the laboratory is:

$$\varepsilon_{exp} = 1 - e^{-n_0^{'}} \tag{3.4}$$

The measured efficiency is smaller that the theoretical one because the lowest value achievable for the threshold of the discriminator is limited by the noise level and the avalanches that induce signals compatible with noise can not be measured. Furthermore, there is always a probability that the electrons in a cluster are attached and no electron signal is collected.

3.2.2 Time response

There is a model [40] that explains the main dependencies of the intrinsic time response of an RPC. It allows to obtain the time response function in terms of $n_0^{'}$ (related to the measured efficiency) and the growth coefficient $S = (\alpha - \eta)v_e$ (α is the Townsend coefficient, η is the attachment coefficient and v_e is the drift velocity):

$$\rho_T(t) = \frac{n_0^{'}}{e^{n_0^{'}} - 1} \frac{e^{(\tau_{th}-St)-\exp(\tau_{th}-St)}}{\sqrt{n_0^{'} e^{(\tau_{th}-St)}}} I_1 \left(2\sqrt{n_0^{'} e^{(\tau_{th}-St)}} \right) \tag{3.5}$$

where τ_{th}=ln[m_t(1-η/α] and I_1 is the modified Bessel function. The rms[2] (time resolution) can be extracted from Eq. 3.5:

$$rms_T = \frac{K(n_0^{'})}{S(V)} \tag{3.6}$$

$K(n_0^{'})$ has an analytic expansion as function of $n_0^{'}$ that can be found in [41]. Therefore, the time resolution can be separated in two different contributions: on one hand, the fluctuation due to the primary and multiplication statistics $K(n_0^{'})$ that depends on the primary interacting particle and, on the other hand, the growth coefficient of the gas S that depends on the applied field and the particular gas mixture. The effect of τ_{th} in Eq. 3.5 (equivalently, the threshold of the discriminator) is just a global shift that will not affect any moment of order larger that one around the mean of the distribution, in particular the time resolution.

The maximum field applied in a timing RPC is limited by the apparition of streamers, that start to deteriorate the capabilities due to the large charge released. In a first approach, this situation can be identified with the Raether condition $\alpha g \simeq 20$ [42] (where g is the gain of the detector), which is an experimental limit for the maximum gain attainable in wide gaseous detectors before the streamer can progress:

$$m = e^{\alpha g} \simeq e^{20} = 5 \times 10^8 \tag{3.7}$$

this is called *Raether limit*. Replacing α in Eq. 3.6, it is possible to infer that the best time resolution achievable in a given configuration behaves as:

[2]Root Mean Square.

$$rms_T|_{min} \sim \frac{K(n_0^{'})}{v_e} g \tag{3.8}$$

The dependence on the gap size is also present through the number of primary clusters $n_0^{'}$ but, being this dependence relatively small [22], the dominant effect is that the time resolution worsens with the increase in the gap size. This effect is well established experimentally [34], showing deviations for very small gaps (g<0.3 mm).

Eq. 3.5 has tails towards delayed times, becoming gaussian for high $n_0^{'}$. In this limit, $K(n_0^{'}) \simeq \frac{K}{\sqrt{n_0^{'}}}$, [22]), and Eq. 3.8 can rewrite as:

$$rms_T|_{min} \propto \frac{1}{v_e(E)} \sqrt{\frac{\lambda g}{N}} \tag{3.9}$$

being v_e the drift velocity at the field corresponding to the beginning of the streamers, g the gap size, N the number of gaps and λ the mean free path for ionization.

3.2.3 Time-charge correlation

As it was explained above, Eq. 3.5 stands for the intrinsic response of the RPC and no attempt is done to describe the extra jitter coming from the electronics. Besides the unavoidable electronic jitter, a systematic shift of the time of flight (tof) measured at fixed velocity of the primary particle is always present and it depends on the avalanche size. This shift can be subtracted, if the charge is measured, through a procedure called 'slewing correction'.

There is a part of the time-charge correlation coming from electronics, but it has been suggested also that there is an intrinsic correlation coming from the avalanche physics [37]. Typically, the slewing correction allows to improve the time resolution by 20-60 ps (see Table 3.2 and Fig. 7.47).

3.2.4 Space-charge

Space-Charge is crucial for interpreting the charge spectra and efficiencies of both RPCs [43] and tRPCs [44]. It reduces the released charge by several orders of magnitude as compared to the one expected from a proportional regime. Moreover, it allows to reach very high values of α before streamers start to be important, resulting in a very narrow time response (Eq. 3.6).

The avalanche grows until reaching a critical number of electrons, related to the situation where the avalanche self-field is comparable to the applied one, resulting in a reduction of the effective field in a large region of the avalanche development. Further ionizations are highly reduced for a large fraction of the secondary electrons. The average field created by the avalanche is proportional to the number of carriers (neglecting diffusion effects):

$$\overline{E}_{avalanche} \propto \overline{n}_e \propto \overline{q} \tag{3.10}$$

According to the assumptions made, the avalanche will grow up to the point the local field is equal to the applied field E, $\overline{E}_{avalanche}$=E. This implies that $\overline{q} \propto E$. In a parallel geometry $E \propto V$ and therefore:

$$\overline{q} \propto V \tag{3.11}$$

For low voltages, i.e., before the onset of the Space-Charge regime, the growth of the average charge $\overline{q}$ with V will be the one expected for a proportional counter:

$$\overline{q} \propto e^{\alpha(V)g} \tag{3.12}$$

For high fields, the behaviour of α as a function of V can be approximated by a linear trend [45], so the growth of the $\overline{q}$ with V is well described by an exponential.

3.2.5 Prompt charge vs induced charge

The charge induced during the drift of the electrons along the gap is denoted as prompt/electronic charge q_{prompt}, a process that takes place in the first 3 ns after cluster formation ($v_e \simeq 100$ μm/ns, $g/v_e \simeq 3$ ns). The drift time of the ions is considerably larger, at the level of μs. The *induced charge* $q_{induced}$ is used to denote the charge induced during both the drifts of the electrons and the ions of the gap.

The total charge released, denoted as the *total charge* q_{total} or simply q, cannot be accounted for before the flow in the resistive plates takes also place (at the scale of its relaxation time). The average ratio $\overline{q}_{prompt}/\overline{q}_{induced}$ is often evaluated, as it has a dependence in the case of a parallel plate chamber in the proportional regime:

$$\frac{\overline{q}_{prompt}}{\overline{q}_{induced}} \simeq \frac{1}{\alpha g} \tag{3.13}$$

indicating that most of the collected charge is induced during the ions drift, as these are mainly produced close to the anode, drifting along the whole gap g. In the presence of Space-Charge effects, the ratio is modified and different descriptions of this regime can be evaluated [44].

3.2.6 Electronics in tRPCs

The fast signals induced in the readout electronics of the tRPCs have rise-times at the level of the ns. Then, very fast amplifying electronics are required, with a bandwidth up to 1-2 GHz [46], [47]. A detailed description of the acquisition electronics of the tRPCs of the HADES wall will be done in this work but, previously, a brief description of different Front-End Electronics (FEE) developed for other tRPC walls will be introduced.

Table 3.1 shows a comparison between the performances of these FEE designs of the main experiments which have been developed timing RPC walls: HARP [48], ALICE-NINO [49], [50], STAR [51], [52], FOPI-TACQUILA [53], [54], [55] and HADES [56], [57]. Most detailed features are the following:

Detector FEE	HARP	ALICE-NINO	STAR	FOPI-TACQUILA	HADES
$N_{channels}$ (detector)	368	160000	23000	5000	2000
N_{boards}	2	1	1	2	2
$N_{channels}$ (board)	8	8	24	16	4
preamp factor gain	30	-	-	200	40
preamp gain [dB]	29	-	-	-	35
preamp bandwidth	440 MHz	250-500 MHz	560 MHz	1.5 GHz	1-2 GHz
digital output	ECL	LVDS	ECL	PECL	LVDS
power consumption	-	40 mW/ch	-	500 mW/ch	500 mW/ch
σ_T (FEE) [ps/ch]	15	20	32	18±3	16±3
σ_T (TDC) [ps/ch]	35	20	40	12±2	40±5
σ_T (total) [ps/ch]	26	-	42	≤33±4	≤40±5

Table 3.1: *Comparison between the FEE of different timing RPC walls and their characteristics (see references below).*

- The FEE of the tRPC wall of HARP [48] consists on two different boards: an 8-inputs summing preamplifier (with a gain factor of 30 and a bandwidth <1 GHz) and a 16-channel module splitter shaper-discriminator with an ECL[3] output. Connected to these boards there are a TDC (35 ps) and a QDC[4] (0.1 fC), both modules from CAEN. The time resolution per channel of the FEE is σ_T=15 ps and including the whole chain with the TDC is σ_T=26 ps.

- The NINO ASIC[5] of the ALICE group [49], [50] is a single chip with a differential input and it is characterized by its very low power consumption of 40 mW/channel. It has a high-bandwidth transimpedance amplifier step (δf∼250-500 MHz), implementing a measurement of the Time-over-Threshold (ToT) in the digital LVDS[6] output signal, for performing the slewing correction. The ToT width is sampled with a multi-channel "High-Performance TDC" (HPTDC) ASIC [58] of 25 ps bin, developed at CERN for the ALICE group. This IC allows for a measurement of both the leading and trailing edge, obtaining for the NINO a time resolution σ_T=20 ps/channel.

- The FEE of the tRPC of STAR [51], [52] consists on one board (TFEE), including preamplifier (a 560 MHz bandwidth transimpedance amplifier) and discriminator steps to accommodate 24 pad signals. The ECL output width implements the ToT for the slewing correction. The HPTDC is implemented in other board (TDIG) to measure both the leading edge and the width of output signal, obtaining for the TFEE a time resolution σ_T=32 ps/channel and for the whole chain a σ_T=42 ps/channel. A TCPU board functions as a data concentrator.

[3]Emitter Coupled Logic.
[4]Time to Digital Converter and Charge to Digital Converter.
[5]Application-Specific Integrated Circuits.
[6]Low Voltage Differential Signal.

- The TACQUILA board [54], [55] of FOPI is only part of the electronic chain, directly connected to the FEE board, a highly integrated 16-channel card [53]. This FEE board has a time resolution $\sigma_T \leq 18$ ps, a crosstalk between channels less than -43 dB and a power consumption of 0.5 W/channel. TACQUILA works with the digital signals after the amplification (with a maximum gain of $G \sim 200$ at a bandwidth of $\delta f \sim 1.5$ GHz) and the discriminator stage. The PECL[7] output of the discriminator is sent to the TACQUILA, which is a 16-channel board started by any of the channels and common-stopped by a free running 40 MHz clock, yielding a very low jitter of $\sigma_T = 12 \pm 2$ ps/channel. The FEE electronics stage rises the jitter up to $\sigma_T = 33 \pm 4$ ps/channel, within the requirements for operate a timing RPC. The charge for the slewing correction is measured in a external QDC.

- The FEE of the HADES RPC wall, that is the aim of this work, will be described in the next chapters. The FEE is split on two boards [56], [57] and it is a fast (with a gain of $G \sim 40$ at a bandwidth of $\delta f \sim$1-2 GHz) and compact low-noise FEE electronics that use the ToT information over the LVDS output signal for the slewing correction. The power consumption is 500 mW per channel.

3.2.7 Examples of timing RPC walls

In this section, the different timing RPC walls, in construction stage or already finished that have been developed, are described. The main experiments that are applying this technology to the field of nuclear and particle physics are the same experiments of the section 3.2.6: HARP [59], [60], ALICE [31], STAR [51], [61], [63], FOPI [54], [32] and HADES [3], [64], [65], although others like CBM [66] foresee to use this technology for the future.

Main features of these timing RPC walls are presented in Table 3.2, allowing to compare their performances. Some of the fields require explanation: the efficiency do not include geometric inefficiency, it stands for the intrinsic efficiency of the device. The 'cell size' is defined as the area per pick-up pad/strip and stands for the typical values. The rate capability is difficult to obtain: in HADES and ALICE it has been defined as the rate required for a 5% drop in the efficiency, and HARP and STAR are just reasonable estimates from data. Finally, some entries are empty, meaning that the magnitude has not been published. Furthermore, not all the measurements were taken under the same conditions. HARP data really come from the final barrel already installed, ALICE represents the performances under spot illumination, validated during the commissioning in 2008, STAR tested a single tray under realistic conditions and both FOPI and HADES are already tested the commissioning and installed, although FOPI have already started its physics program.

[7] Positive Emitter Coupled Logic or Positive ECL.

Detector	HARP	ALICE	STAR	FOPI	HADES
N_{gaps}	4	10	6	8	4
gap size [mm]	0.3	0.25	0.22	0.22	0.3
gas [$C_2F_4H_2$/SF_6/iso-C_4H_{10}]	90/5/5	90/5/5	90/5/5	85/10/5	90/10/0
electric configuration	an-cat-an	an-cat-an	an-cat	an-cat-an	an-cat-an
cell size [cm×cm]	22×10.6	2.5×3.7	6.3×3.1	90×4.6	60×2
detector size	10^2	150 m^2	60 m^2	5 m^2	8 m^2
$N_{channels}$ (detector)	368	160000	23000	5000	2000
HV/gap	3 kV	2.4 kV	2.35 kV	3.3 kV	3.2 kV
ε	99%	99.9%	95-97%	99%	99%
plateau length	300 V	2000 V	500 V	600 V	400 V
σ_T [ps/ch]	-	90	120	-	100
σ_T [ps/ch] (after slewing corr.)	150	40	60	60	73
crosstalk/neighbour	<10%	-	-	-	<2%
3-σ tails	-	-	-	<2%	2%
experiment rates [Hz/cm^2]	1		10	50	700
dark rate [Hz/cm^2]	<0.1	-	<0.3	<1	2-3
rate capability [Hz/cm^2]	≤2000	≤1000	-	-	350
resistive material	float glass	float glass	float glass	float glass	float glass

Table 3.2: *Comparison between different timing RPC walls, showing some of their characteristics (see [22] and references below).*

HARP

Located at the T9 beam of the CERN-PS, the tRPC wall of the HARP experiment [59], [60] is the first timing RPC wall to operate in a HEP experiment (it took data in 2001 and 2002) and the only one finished so far. The RPC system was designed to measure TOF for particle momenta in the range of a few hundred MeV with a time resolution of σ_T<200 ps (for PID[8]) which is considered adequate despite the short particle flight distances of 0.5-2 m. In line with the goal to measure differential cross-sections at the 1.2% level, the detection efficiency was required to be ∼99%. There were no particular requirements on rate capability and spatial resolution given the low event multiplicities in HARP (<1 Hz/cm^2).

The design and construction of the whole cells (368 channels) and the electronics was done between December 2000 and April 2001. It is based on the original design [35], consisting in 4 gaps, 0.3 mm wide, operated at 3 kV/gap, with resistive plates made of standard float glass in a double layer configuration for avoiding geometric losses. The chambers operated with a gas mixture similar to the 'standard' [38], $C_2F_4H_2$/SF_6/iso-C_4H_{10} in a proportion 90/5/5. The glass has a thickness of 0.7 mm with a specific resistance of ∼10^{13} Ωcm, over an area of 192×10.6 cm^2 per tRPC module, being each module divided in 64 pads, grouped in 8 strips per FEE channel.

Typical efficiency is at the level of 99% and time resolutions around 150 ps, that can be reduced to 105 ps for a single pad. Crosstalk was reported below the level of

[8]Particle IDentification.

10%. Although rate capability was not a tight requirement, a test was performed at Φ=2 kHz/cm^2 at CERN-PS, observing a slight deterioration of the performances.

ALICE

The construction of the ALICE tRPC wall [31] was foreseen in 2000 in the framework of the new Large Hadron Collider facility (LHC) at CERN. One of the techniques used by ALICE for PID is the measurement of their time of flight, which combined with the particle momentum and track length, gives the particle mass. It provides the best performances so far.

ALICE is a huge project for covering 150 m^2 with 160000 electronic channels and a time resolution below 100 ps, with a high overall efficiency. The detector element is a long MRPC (up to a total of 10 gaps of 250 μm) with 96 readout pads of 2.5×3.7 cm^2 arranged in two rows, with an applied voltage V=2.5 kV/gap. The voltage is lower than HARP (see Table 3.2) because the gap is also slightly smaller, requiring less voltage for getting the typical operating fields of 100 kV/cm. The resistive plates are commercial glass as thin as 400 μm.

This MRPC design completely satisfy the requirements of the ALICE TOF wall, providing an efficiency up to 99.9%, resolutions better than 50 ps and an excellent rate capability around 1 kHz/cm^2. During the end of 2007 and 2008 the construction and commissioning of the whole project was done [67].

STAR

The tRPC wall for STAR [51], [52], at RHIC was born at CERN with some of their members coming from the ALICE tRPC group. This TOF detector replaces the existing 120 trays of the Central Trigger Barrel (CTB). Its main technical requirement is to provide a time resolution below 100 ps over a large area of 60 m^2. The detector is constituted by modules of 9.4×21 cm^2, picking up the signals in pads of 6.3×3.15 cm^2. It is made of 6-gap tRPCs of thin glass (550 μm) and very narrow gaps of 220 μm, allowing the operation at ±7.5 kV between the electrodes.

Tests with a pulsed beam (0.3 ms) at CERN-PS seem to guarantee performances at the rates of around 10 Hz/cm^2 expected for the STAR experiment. The efficiency is at the level of 95-97%, plus additional 5% losses due to geometric inefficiency. Regarding time response, 60-70 ps of resolution were achieved, fulfilling the requirements. Furthermore, measurements under a pulsed beam gave an idea that the rate capability could be higher than 500 Hz/cm^2 and other in-beam measurements for p-p and d-Au collisions have shown also good performances [63].

FOPI

FOPI detector [32] is located at GSI-SIS in Darmstadt (Germany). During the last years a ToF wall based on Multi-strip MRPCs [33], [35] has been developed as an upgrade of the existing detector. The ToF barrel has an active area of 5 m^2 with

2400 individual strips (900×1.6 mm^2) which are readout on both sides by a custom designed electronics [53], [54]. The detector design is segmented in a 16 strip anode Multi-strip with an active surface of 4.6×90 cm^2. They use eight gaps defined by 220 μm finishing the line in a double stack configuration (2×4). The anode is placed in between the two glasses. This configuration allows to operate the counters at a moderate high voltage $U_{RPC}\leq$9.6 kV at a high electric field ($E\leq$109 kV/cm).

The cells are optimized for a single-ended readout electronics with an input impedance of 50 Ω. To minimize the internal reflection probability and the signal losses due to impedance mismatch the signal path was adapted to 50±3 Ω [68].

First developments with 6-gap tRPC (0.3 mm) have reached efficiencies of 97±3% and time resolutions of 73±5 ps [32], using the standard mixture. Its performance has been tested under different conditions: ^{60}Co, proton and deuterium at rates of 50-100 Hz/cm^2. The final tests of mass produced Multi-strip MRPCs showed that the best performance is reached between 1 and 150 Hz/cm^2 with efficiencies above $\varepsilon\geq$99% at time resolutions $\sigma_T\leq$60 ps at an electric field $E\geq$107 kV/cm [68]. The system resolution for the electronics is $\sigma_e\leq$25 ps. The ToF barrel was installed and commissioned in 2007 and FOPI's physics programm started.

3.3 The HADES tRPC wall

HADES, also located at GSI-SIS, is investigating the properties of Nuclear Matter induced by p, nucleus and π beams at kinetic energies in the range of 1-3.5 GeV/A [3]. To deal with the high particle multiplicities (rates of $\Phi\leq$700 Hz/cm^2) expected at that range of energies with heavy nuclei systems, such as Au+Au, and for lighter nuclei systems at the energies of up to 8 GeV/A to be provided by FAIR, the HADES ToF wall was upgraded with a timing RPC wall. As the main part of such upgraded project, the TOFino wall has been replaced by a new high granularity ToF wall based in timing RPC detectors. The design of this ToF wall was developed by Dr. D. Gonzalez-Díaz in his thesis [22]. A summary of the design will be explained in this section, together with the construction and the installation of the wall.

3.3.1 Specifications of the ToF wall

In order to know the environment of the RPC wall inside the spectrometer, Fig. 3.3 shows a lateral profile of one of the six HADES sectors, focused on the detectors close to the tRPC wall: a) the outer drift chamber (MDC IV), b) the large angle scintillator TOF wall and c) the three planes of the Shower detector. The values 12° and 45° have been extracted from the geometry implemented in the HADES simulation package (from the limits of the active volume of the TOFino wall that was placed at the tRPC position). As is shown in Fig. 3.3, the 'laboratory' reference system has its origin placed at the nominal target position (vertex), with Z defined along the beam axis, being positive in the downstream direction, and Y

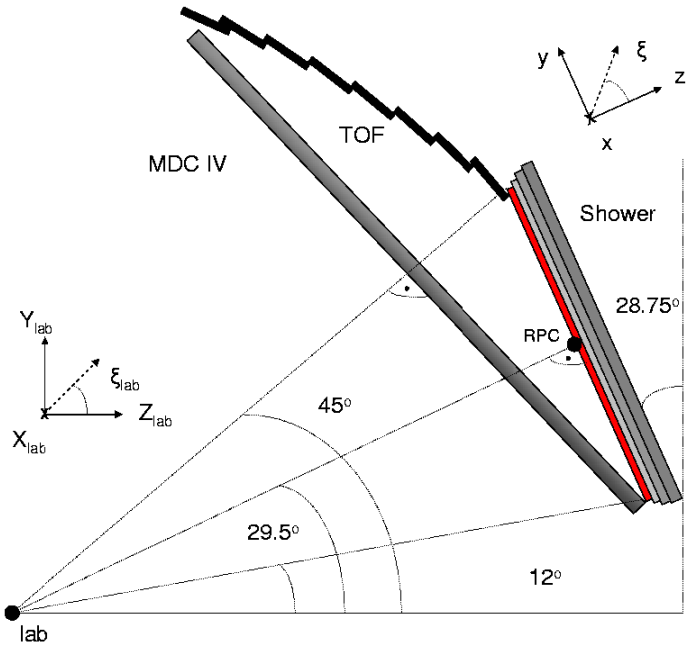


Figure 3.3: *Situation of the tRPC wall in the HADES spectrometer [22].*

defined perpendicular to the floor, upwards. The HADES geometric acceptance in this reference system ('lab') can be expressed in spherical coordinates as:

$$18^\circ < \theta_{lab} < 85^\circ \tag{3.14}$$

together with roughly 360° coverage on the azimuthal coordinate ($0^\circ < \Phi_{lab} < 360^\circ$), grouped in six identical sectors as the rest of the HADES detectors. The other reference system, called 'local' (denoted in lower case and placed in the tRPC), is also shown in Fig. 3.3. The origins of both systems are represented by circles.

The tRPC wall must cover the low polar angle region from 12° to 45° in order to meet HADES geometric acceptance and, practically, the whole azimuthal area. The small angle 12° (see Eq. 3.14) arises from the necessity to measure positive charged tracks that are bent towards low θ_{lab}. Each sector covers approximately 1.3 m^2 (a total area of $\sim$8 m^2) and it is placed over the Shower detector and both will mechanically attached to the same frame (see Fig. 3.3 and 3.13).

The design of the HADES ToF wall at low angles was optimized for handling the highest rates and multiplicities foreseen at the HADES spectrometer, for the maximum energies available at SIS18 (up to 8 GeV/A). On one hand, this means that the wall must be operational for Au beam intensities up to I=10^8 ions/s impinging over a Au target with 1% interaction probability, according to the technical proposal [3] (for technical reasons it was decreased to I=2×10^7). On the other hand, the detector must have enough granularity to cope with the highest multiplicities foreseen (central Au+Au collisions with a kinetic energy E_{kin}=1.5 GeV/A).

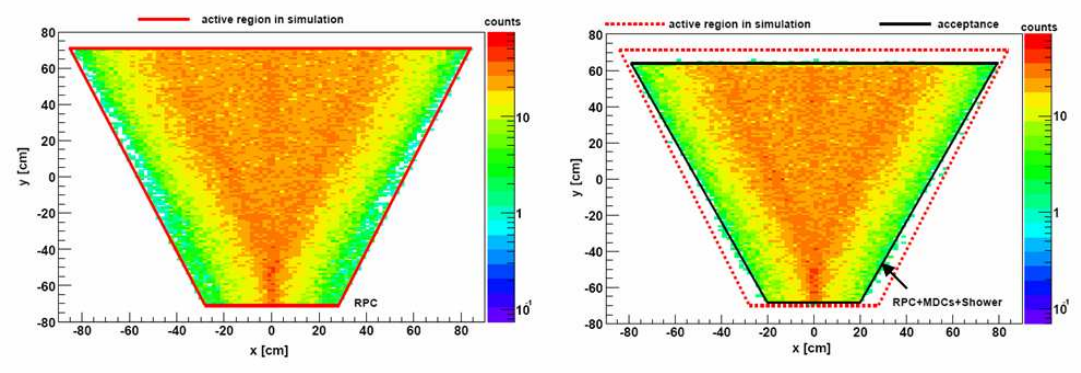


Figure 3.4: *Left: figure showing the illuminated for acceptance estimates under a primary distribution that contains all the possible tracks within the spectrometer. Right: the same distribution but requiring a valid hit in all the drift chambers and the Shower ([22]), providing an estimate of the acceptance (black line).*

Taking into consideration the HADES overall performance, the inner ToF wall should conform to the following parameters [22], [65], [69]:

- Area of the ToF wall $\sim$8 m^2.
- Occupancy per cell below 20%, recommended below 10% for lepton detection.
- Rate capability up to 1 kHz/cm^2 in the innermost part for higher intensities.
- Granularity determined by a robust multi-hit capability, with a hit-loss probability below 20% for the heaviest system considered.
- High time resolution ($\sigma_T \simeq$100 ps) for separating e^+e^- pairs from fast pions [70], together with low crosstalk.
- High both intrinsic and geometric efficiency, close to 100%.
- It must be equipped with fast, low noise, compact and robust FEE for operating a large number of channels under stable conditions.

3.3.2 Characteristics of the tRPC wall

A simulation for nucleus-nucleus collisions producing a particle distribution over a plane at the tRPC wall position was developed in [22]. Some results are shown.

Acceptance

The geometric acceptance of the HADES spectrometer at the tRPC position has been defined by generating all possible tracks over it, imposing the condition that

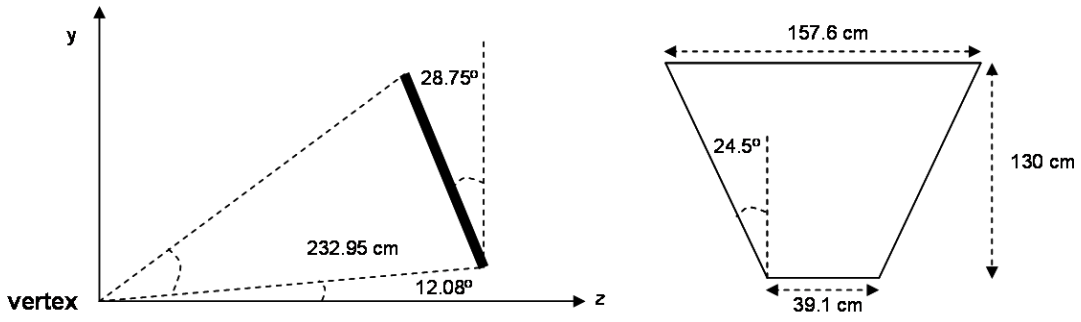


Figure 3.5: *HADES acceptance at the tRPC in the laboratory reference system.*

such track provides a valid hit in all the MDCs and the Pre-shower (ideal MDC and Pre-shower response is assumed).

The distribution obtained over the tRPC is shown in Fig. 3.4. The tRPC area has been chosen in simulation to be larger than the active area of the Pre-shower detector. In the left side of Fig. 3.4, the distribution of all tracks over the tRPC is shown, while, in the right one, the same distribution is shown after imposing the condition of having a valid hit in the 4 MDC planes and the Pre-Shower, therefore defining the limits of the geometric acceptance.

The dimensions of the HADES geometric acceptance obtained from Fig. 3.4 are shown in Fig. 3.5, together with its position in the 'lab' reference system. For design purposes, the geometric acceptance is defined at the plane of the foreseen last gap of the RPC in the downstream direction.

Expected rate

The primary intensity considered is $I{=}2{\times}10^7$, corresponding to the maximum value expected in HADES for a heavy ion environment. The interaction probability in the target was set to 1% according to HADES proposal [3] and primary Au+Au collisions at 1.5 GeV/A were generated. The rate expected at the tRPC wall as a function of y (averaged over x) is shown in Fig. 3.6-left.

It can be observed that the distribution is peaked towards low values of y (low polar angles θ_{lab}) due to the Lorentz boost. The strong dependence of the rate with y[9], suggest that different kind of tRPC could be used within the same experiment [66], for covering different polar angles. According to previous works on glass timing RPCs [37], [71], the expected maximum rate ($\Phi{\simeq}700$ Hz/cm^2) is already at the limit where glass tRPCs can offer good performances.

Besides the rate limitation, related with the accumulation of charge over the resistive plates [22], working at high rates also results in an increased probability of pilling-up of the tRPC signals. For an estimate of this effect, it must be re-

[9]A factor $\times 10$ reduction is observed from the lower value of y ($\theta_{lab}{\sim}12°$) to its maximum value ($\theta_{lab}{\sim}45°$).

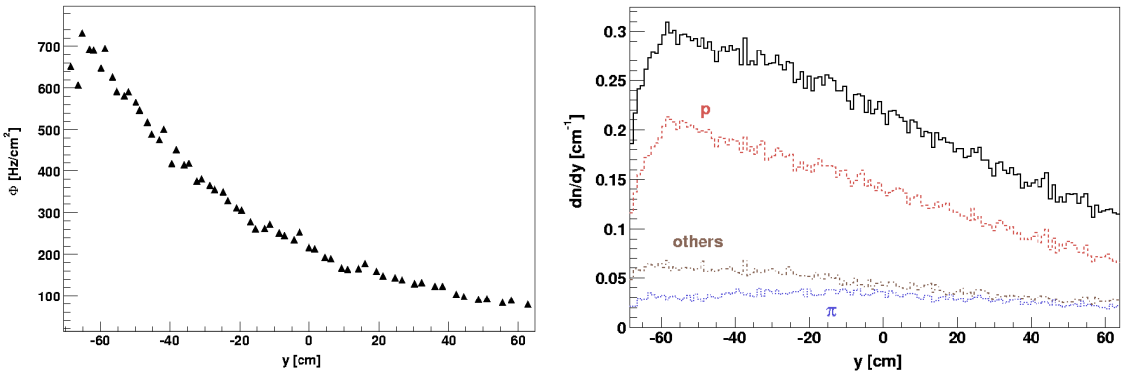


Figure 3.6: *Left: rate over the tRPC wall for the most unfavorable environment expected at HADES, minimum biased Au+Au collisions at 1.5 GeV/A, $I=2\times10^7$ ions/s, $P_{int}=1\%$ and $B=0.72\times B_{max}$. A maximum value $\Phi=700$ Hz/cm^2 is reached at the lower polar angles. Right: occupancy density at the tRPC wall (full line) for the same environment. The contributions of protons (dashed), pions (dots) and others (dash-dotted) are also shown, being the latter dominated mainly by electrons. The reduction of the number of protons at low y is caused by the MDC frames (pictures from [22].*

called that the tRPC signal extends in time up to around $\Delta T_{signal}\sim1$ μs, mainly due to the ionic tail. Then, if the frequency of hits over the tRPC cell is larger than $1/\Delta T_{signal}\sim1$ MHz, the pile-up becomes important, resulting in a worsening of the timing performances. For the highest rates expected at low polar angles ($\Phi\simeq700$ Hz/cm^2) and the typical cell sizes of that region (around 15×2 cm^2, see next sections), the frequency of hits is kept as low as 0.020 MHz, that guarantees a safe operation with pile-up at the level of 2%.

Occupancy

The occupancy density is the average number of tracks over the tRPC acceptance per primary interaction per unit length along the y direction. Fig. 3.6-right shows the occupancy for the highest multiplicity environment expected in HADES: central Au+Au collisions at 1.5 GeV/A, yielding $N=30\times6$ charged particles over the tRPC.

According to Fig. 3.6-right, HADES requirements of 10-20% occupancy per cell can be fulfilled, at low y, by strips having widths in the range 3-6 mm (similar to FOPI experiment). However, the large cluster sizes observed require dedicated multi-hit studies [55]. The cluster sizes can be reduced virtually to one by working with electrically isolated tRPC cells, by the feasibility of producing long cells with widths lower than cm is mechanically questionable.

So, it was decided to keep the cell width at the cm scale, and the required occupancy levels can be obtained by an additional segmentation of the sector in small sub-sectors or columns (Fig. 3.7 shows different possibilities). The advantages of a moderate segmentation (therefore wider cells) are considerable [22]. Each seg-

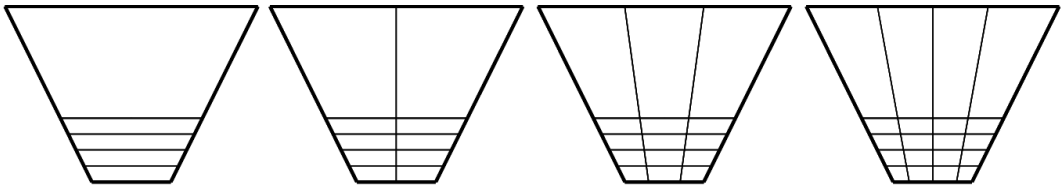


Figure 3.7: *tRPC wall segmentations in 1-4 columns that keep constant the area of the cell and provide, in a first approach, equivalent occupancies and granularities.*

mentation produces an inefficient region due to the separation between the tRPCs columns, that reduces the geometric acceptance. Then, a large number of columns is not advisable. On the other hand, by symmetry, an even-fold segmentation places an inefficient region at the middle of the sector, a zone where an important fraction of the low momentum particles is strongly focused at the tPRC plane [22], [72] due to the inhomogeneities of the magnetic field.

3.3.3 Design and construction of the ToF wall

1-layer layout

According to the arguments presented in previous section (see more details in [22]), a 3-fold segmentation with cells electrically isolated, each of them featuring a width that provides an homogeneous occupancy $n \simeq 20\%$ in the most unfavorable scenario expected in HADES, is a reasonable choice, due to the following reasons:

1. The electric isolation provides robust multi-hit performances by construction (crosstalk levels below 1% were obtained for the first prototype tested in 2003 [64], [65], [22]).

2. The width of the cells can be kept at the level of $\Delta y \simeq 2$ cm for the lower polar angles, fulfilling the occupancy criteria ($n \simeq 20\%$).

3. The shorter lengths as compared to the case of single segmentation reduces significantly the probability of a coincidence of a particle and a lepton in the same cell. Moreover, the probability of having a clean lepton signal is around 90% for the configuration presented [22].

4. There is no loss in efficiency towards the middle of the sector.

The problem of this configuration, as said before, is a 1-layer layout constituted by electrically isolated cells requires some spacing between the active volumes of each cell for placing the shielding. Such an approach has been implemented through the use of aluminum profiles. Results of the prototype test developed at 2003 [22] indicate that the loss in geometric acceptance can be almost 15% for perpendicular incidence, even in the very tight configuration chose, where the active regions were separated by only 3 mm.

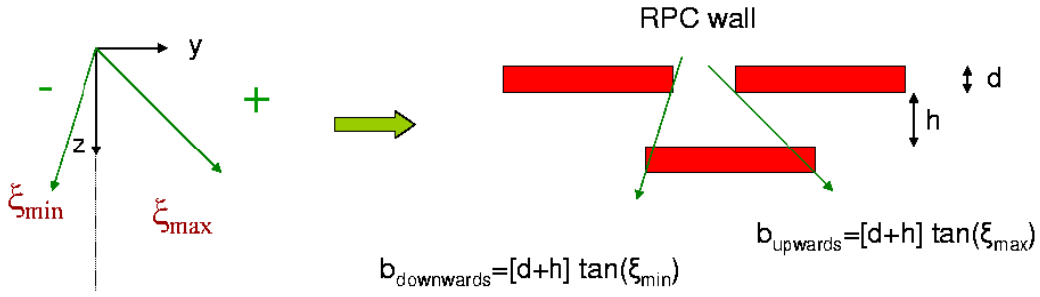


Figure 3.8: *Relation between the extreme values of the projected angles at the position of the tRPC wall and the required overlap.*

2-layer layout

For avoiding dead regions, the use of a 2-layer configuration is chosen. The overlap required is given by the angle of incidence of the particles at the tRPC position (see Fig. 3.8). The overlap was determined in a such a way that all the possible tracks within the spectrometer coming from vertex and with a momentum between 100 MeV and 1000 MeV go through, at least, four tRPC gaps (providing an $\varepsilon \geq 99\%$). Therefore, the maximum and the minimum angles ξ at each position y within the tRPC wall provide the required overlap (Fig. 3.8):

$$b_{downwards}(y) = (d + h)\tan[\xi_{min}(y)] \tag{3.15}$$

$$b_{upwards}(y) = (d + h)\tan[\xi_{max}(y)] \tag{3.16}$$

where d is the active thickness of the detector (region comprised between the two outermost gaps of each 4-gap cell, d=0.72 cm) and h the separation between active volumes of different layers (assumed to be 1 cm due to mechanical constraints).

For simplifying the design, other parametrization was also done: in the lower part of the sector, the change in the overlap as a function of y can be implemented as a global shift of 1 mm of all the cells in one layer every 10 cm along the y direction.

3-D design

From the discussions of previous sections, a convenient design was made based on the cell dimensions and the overlap between layers [22]. The detector is composed by individually shielded strip-like RPC cells, organized in two partially overlapping layers. To avoid excessively narrow strips, which might be dominated by edge effects, each sector was divided in three columns (see upper plot of Fig. 3.9), keeping the needed granularity while allowing for wider cells. Then, each layer is composed by 31 rows and three columns, ranging the widths of the cells between 2.2 and 5 cm and the lengths between 12 and 52 cm [69], being the ones placed in the lower polar angle region smaller than the ones placed in the bigger area (from 18° to 45°).

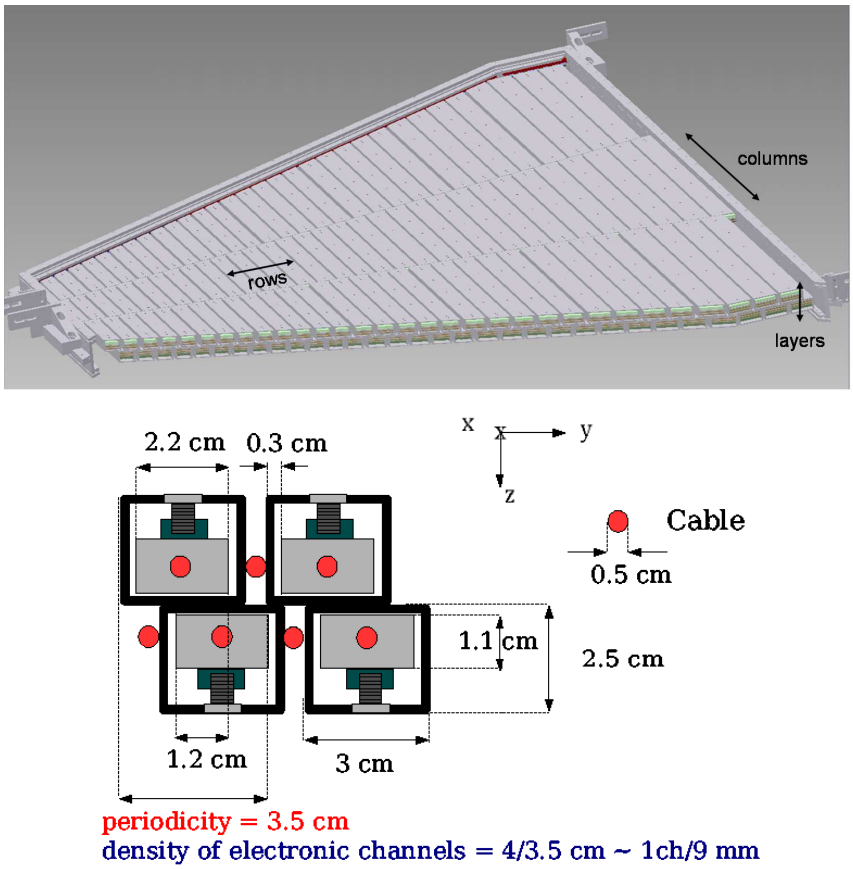


Figure 3.9: *Up: drawing of the internal structure of one HADES RPC sector and also parts of the gas box. The detector is composed by individually shielded strip-like cells, organized in two partially overlapping layers with 31 rows and 3 columns each. The cells variable width matches the expected local particle density. Down: detail of the tRPC cells, projected over one of the sides of the detector. Dimensions at the lower polar angle region, cabling space and the density of electronic channels is shown (pictures from [69], [22].)*

This means that the upgraded inner ToF wall will cover a total area of 8 m^2, divided in six sectors of trapezoidal shape (see Figs. 3.5 and 3.7), with 1116 variable-geometry 4-gap (to provide a total efficiency close to 99% with Eq. 3.1), symmetric, timing RPCs [35]. These cells are readout by 2232 time and charge FEE channels [56], [80] (see next chapters for the FEE design). The density of the electronic channels is shown in Fig. 3.9 (down):

$$N_{cells} = 31\ cells \times 3\ columns \times 2\ layers \times 6\ sectors = 1116 \tag{3.17}$$

$$N_{channels} = 31\ cells \times 3\ columns \times 2\ layers \times 6\ sectors \times 2\ sides = 2232 \tag{3.18}$$

Each cell is individually shielded [73] for robust multi-hit performance and optimum use of the FEE channels (crosstalk minimization). The double layer configura-

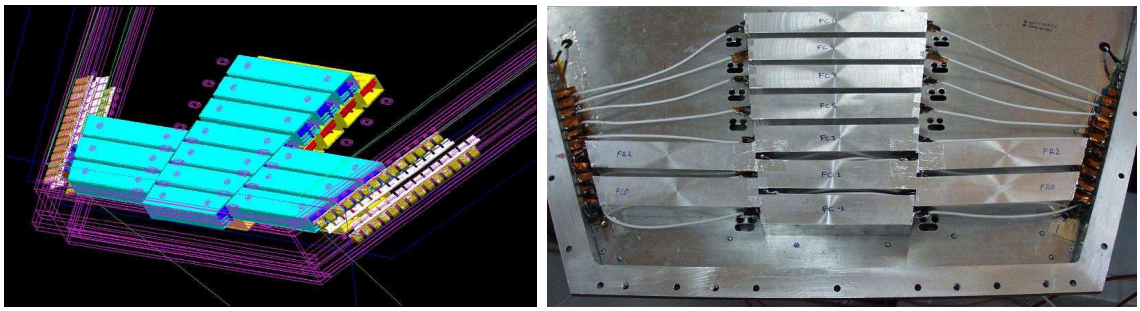


Figure 3.10: *Left: 3D drawing of a detail of the HADES tRPC wall at low angles. Down: shielding profiles that surround the detector cells, showing also the distribution of the signal cables (prototype used in Nov05 test, see chapter 6).*

tion provides a useful [74] degree of redundancy for very accurate tail-free timing [75] of a fraction of all particles crossing the detector. The corresponding 3-D design is shown in Fig. 3.10 for the low polar angle region, together with some of the cells that have been tested in November 2005 [75] (see chapter 6). The asymmetric overlap is visible in the drawing. The chosen way-out of the cables towards the FEE (placed at both sides of the gas box) is also shown in Fig. 3.10 (right).

The individual cells are made of three aluminum electrodes and two glass electrodes, all of 2 mm thickness (Fig. 3.11). The resistivity of the glass is $\rho\sim 2\times 10^{12}$ Ωcm. The gap is defined by PEEK[10] monofilaments of 270 μm diameter, spaced between 5 and 10 cm along the cell. The ensemble is housed inside individual shielding tubes and compressed by the three springs that apply a controlled force to a PVC plate that distributes the force. This layout tries to keep good mechanical uniformity of the gap (any variations above 10% are likely to perturb the time resolution [76]), while minimizing the total glass thickness for optimum count-rate capability.

High-Voltage (HV) close to 6 kV is applied to the central electrode via 330 Ω resistors and high voltage cables, while the outer electrodes are connected to ground (see Fig. 3.11). The glass electrodes are kept electrically floating [77]. Insulation to the shielding tube walls is assured by a triple-layer KAPTON^{TM} adhesive laminate. An end-shield made of aluminum foil is spot-welded on the shielding tubes. The signals are collected by the HV cable and fed out via a 2 nF coupling capacitor and 50 Ω PCB[11] stripline feedthroughs that cross the lateral wall of the gas box. Regarding detector-cable impedance matching, no attempt is made.

Geometric constraints

The geometric integration of the HADES tRPC wall have been implemented during last months of 2009. It is an important issue of the wall design, including the final shape and dimensions of the gas box of the required electronic channels room.

[10] Polyetheretherketone.
[11] Printed Circuit Board.

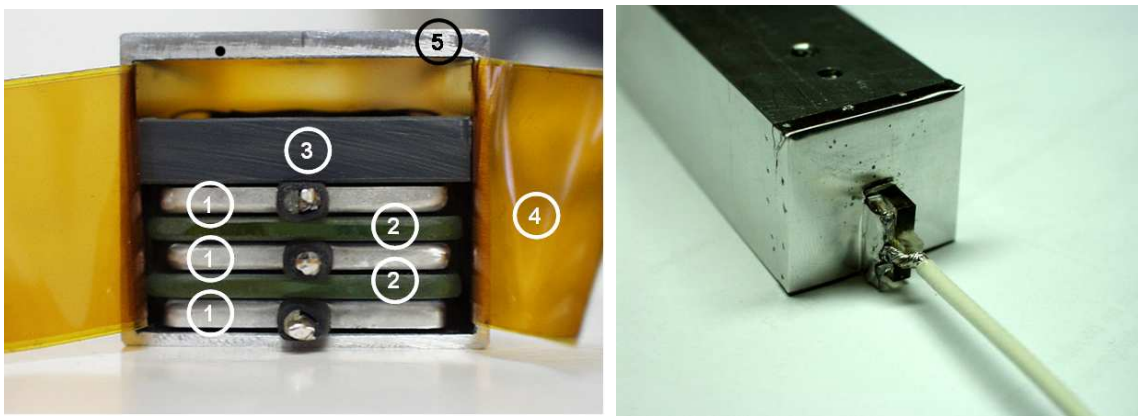


Figure 3.11: *Internal structure of the tRPC cells (left): 1) Al electrodes; 2) glass electrodes; 3) plastic pressure plate; 4) kapton insulation; 5) 2 mm thick Al shielding tube. Finished detector with Al foil shielding end-cap and HV cable (right). HV and readout are connected to the central electrode.*

A full description of all these topics is out of the present work, but let's summarize the three more important geometric constraints [22]:

1. For not coming into conflict with MDC IV frame at the lower polar angles, the tRPC gas box must be not thicker than 10 cm. But this is not a problem in the 2-layer configuration, constituted by 4-gap shielding cells, because the thickness can be kept at the level of 8-10 cm easily.

2. For solving the high proximity between the TOF photomultipliers and the tRPC gas box (see Fig. 3.12-left) at intermediate polar angles ($\theta_{lab}\simeq 45°$), two alternatives were considered: a) to perform a downstream displacement of the set tRPC+shower detector or b) to cut the gas box. Both solutions were evaluated based on CAD designs, resulting in a similar decrease of the geometric acceptance [22] (at the level of 3-4%), distributed in the region of θ_{lab}=40-45°). Due to the similar consequences of both approaches, it was decided to cut the gas box because of practical reasons (see upper plot of Fig. 3.9).

3. The available room for the FEE boards. After fulfilling all the mechanical constraints, the available room renders as small as $\nu\simeq 4\times3\times1$ cm^3 per channel. It was decided to place the FEE boards parallel to the slanting sides of the gas box (see Fig. 6.1), allowing for an easier cooling of the electronics. In that case, the available area per channel is approximately 1×4 cm^2 in the low polar angle region (see down picture of Fig. 3.9). Furthermore, this region is critical for the FEE boards, because the available room between two tRPC sectors is as small as $\sim$1 cm (see Fig. 3.12-right). In order to fit to the available space, the FEE was separated in two different boards (DBO and MBO[12] [56]), placing

[12]DaughterBOard and MotherBOard.

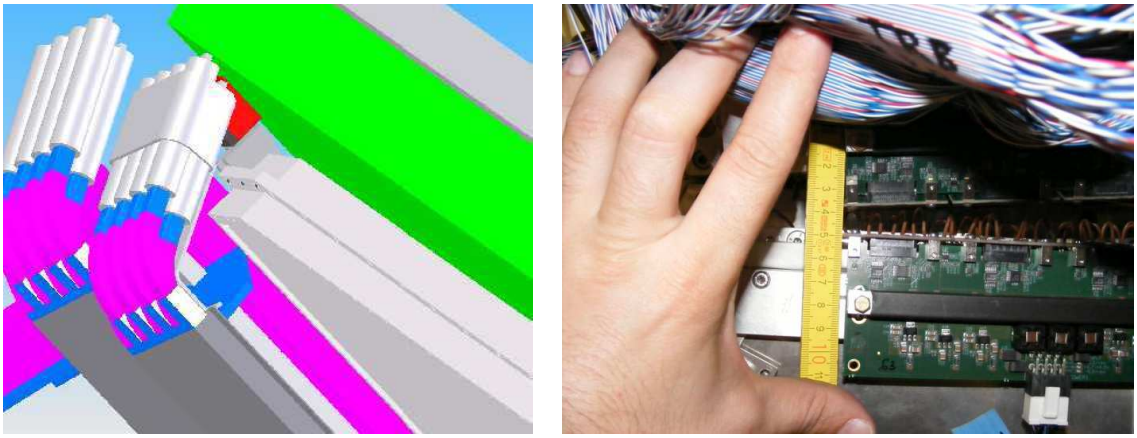


Figure 3.12: *Two critical regions during the HADES tRPC wall installation: i) the region where the gas box and the TOF photomultipliers are closer (left). The picture was done with CAD. The cut in the box is needed for avoiding that both detectors are inter-penetrated. ii) The upper tRPC region, where the room between the FEE boards corresponding to two RPC sectors is ∼1 cm (right).*

voltage regulators, DAC thresholds and test signals in the passive MBO board (see next chapters for a more detailed description). Both FEE boards are assembled in an orthogonal way (Fig. 6.1), being the passive MBO placed over the RPC gas box and the amplification and digitization DBO board keeps parallel to the box.

A picture of the final installation of all the six sectors of the HADES tRPC wall, in their nominal positions over the PreShower detectors, is shown in Fig. 3.13. The FEE position over the RPC box is also shown, together with the LV, acquisition and trigger cabling.

3.4 Conclusions

In this chapter, a general overview of the RPCs gaseous detectors has been presented, mainly focused in the timing RPCs. This technology has been applied to the construction of the HADES tRPC wall covering the low polar angle region $18°<\theta_{lab}<45°$, and the design, the assembly and the installation of the wall are also presented. The cells sizes are set so that the occupancy per cell (double hit probability) is homogeneous along the whole wall, at the level of $n\simeq 20\%$. For that, each sector is divided in three columns and two layers, allowing for reasonable cell sizes.

The wall is constituted by 1116 4-gap tRPC cell electrically isolated. For avoiding the dead regions due to the shielding, a 2-layer scheme has been chosen. The maximum expected rates at HADES in Au+Au collisions at 1.5 GeV/A (Φ=700 Hz/cm^2) are slightly above the ones by ordinary glass timing RPCs.

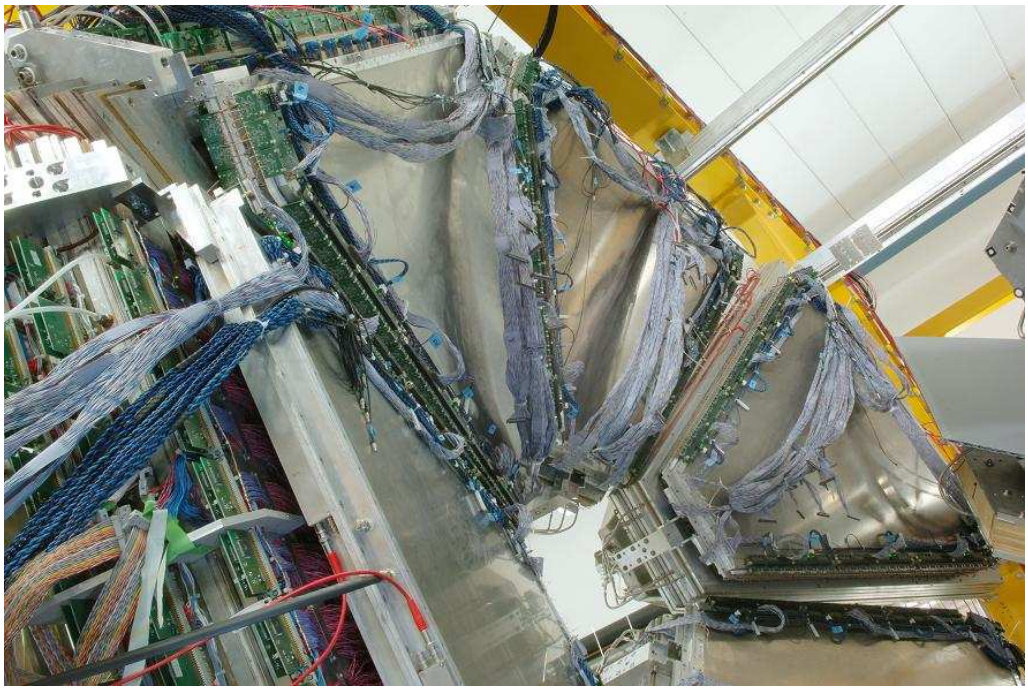


Figure 3.13: *Installation of the full tRPC wall over the PreShower detectors. This is the nominal position of the wall. The FEE structure is slightly visible, together with the cabling.*

The assembly of the wall and the installation in its nominal position in HADES is also presented, showing some of the geometric constraints of the installation.

Chapter 4

Front-End Electronics for the HADES tRPC Wall: first steps

4.1 Introduction of the FEE

This chapter is devoted to explain the main features of the first steps [39] done during the development of the Front-End Electronics (FEE) before the final version of the timing RPCs wall of the HADES spectrometer. As was mentioned in chapter 3, the wall consists on six sectors covering around 8 m^2 in the low polar angle region of the spectrometer. Each sector has 187 shielded cells, distributed in three columns and two layers in each column, with a total number of 1116 RPC cells and 2232 electronic channels [69].

Main FEE requirements for this HADES upgrade were:

- A time resolution in the time-of-flight measurements (tof) $\leq$100 ps rms per channel. For this purpose, precision discrimination of fast rise time input pulses ($\leq$1 nanoseconds) requires amplifying stages performing high gain-bandwidth product (GBW). They preserve the detector time resolution and guarantee the required discriminator sensibility, without sacrifice power consumption and noise performances [46]. For a rise time at the level of $\sim$300 ps a bandwidth of $\sim$1 GHz is needed.

- Time and charge information, both encoded in a single digital signal. This feature reduces the number of electronic channels for acquisition. Also a digital output signal level compatible with the acquisition system is needed.

- A compact and stable design with the minimum number of components (due to small available room) to obtain a moderate power consumption, to avoid noise and to reduce the cross-talk effects.

- A detector efficiency above 95% for single hits at the highest expected rates for the HADES spectrometer ($\Phi \leq 700$ Hz/cm^2).

The development of this FEE consists on three different steps:

1. The first step is the electronic design, including the schematic design and the layout of the boards. The design could be based in a previous simulation and has to satisfy the requirements needed for the detector.

2. The manufacture of several prototypes and the validation tests, including laboratory and detector tests before starting the mass production of the final boards.

3. Test of the manufactured boards before the installation and characterization of the whole system in the experiment.

The different FEE prototypes developed were, chronologically:

- The STEP1 design [39], based in a previous work developed in the LIP of Coimbra [78], one of the groups of the HADES European collaboration: it was a 1-channel in a 2-layer board with two amplifiers steps and an ECL digital output instead of the FEE developed at LIP which was two boards with TTL[1] digital output.

- The STEP2 design [39], [79]: it was a 2-channel and 4-layer board, featuring a LVDS digital output and the Time over Threshold (ToT) algorithm [49], [50] implemented to measure the charge of the RPC signals.

- The STEP3 and STEP4 [80] designs: they were a 4-channel and 6-layer boards with the final size. Both had the same features (a LVDS digital output and the ToT for the charge), except that the STEP3 had two amplifiers and the STEP4 only one and the ECL to LVDS converter.

- The STEP5 [56] and the the final STEP6 board (four channels in six layers each). The main features of both designs are the same, being the LVDS digital output and the 'Charge to Width' (QtoW) algorithm to measure the charge. The differences between both designs are small details, mainly fine tuning of some resistors and capacitors.

In the next sections, the first and the second FEE designs will be presented. Both designs were the first steps developed for the FEE of the HADES tRPC wall. The STEP1 board consisted on two stages: a) the analog part with two amplifier steps and one buffer to send the analog signals to an external ADC[2] to measure the charge and b) the digital part with a ECL discriminator that sends the ECL signal to a TDC to measure the time information. The FEE-STEP2 was an independent design of the LIP FEE. Both designs were developed at the beginning of the project.

[1] Transistor-Transistor Logic.
[2] Analog to Digital Converter.

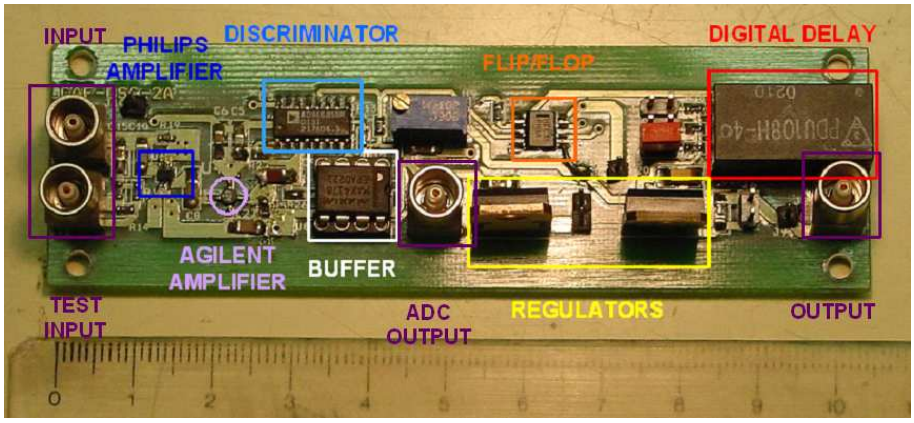


Figure 4.1: *FEE-STEP1 board with one channel. Its size is 10.5×3=31.5 cm^2.*

4.2 The FEE-STEP1 design

As was mentioned before, this first design [39] was an updating of a two boards FEE designed at LIP for the RPC detectors [78], done with the ORCAD [81] program. The main goal of the STEP1 design was to adapt this FEE in only one board and to ECL logic for the output of the digital part. The most important advantage of the ECL logic is that it is the fastest logic because the transistors does not work in saturation mode. But this included a problem: the power consumption is higher for the components in ECL logic. Other disadvantage was the lower number of existing ECL components compared, for example, with TTL logic.

The FEE-STEP1 design [39] consisted of 1-channel in a 2-layer (TOP and BOTTOM) board. All the components were placed in these layers. The board dimensions were 10.5×3 cm^2 (∼31 cm^2), due to geometric reasons for the RPC detector design. The critical dimension was the width (3 cm), because it was the distance between the detector and the keep-in volume limit, approximately. A picture of the STEP1 is shown in Fig. 4.1 where all active components are pointed out.

The FEE-STEP1 board could be divided in three different parts: i) the analog stage with two amplification steps and with one buffer output to measure the charge with an external ADC, ii) the digital step that sends the digital output signal to an external TDC to measure the arriving time of the signal and iii) the voltage regulation. The block diagram of the STEP1 design is shown in Figure 4.2, and both the schematic and the layout are shown, completely, in Appendix A.

4.2.1 Analog and amplification stage

In order to deal with the very high frequencies (GHz range) expected in the tRPC pulses, and continuing with previous works [46], [47], the analog part was based on two high bandwidth Monolithic Microwave Integrated Circuit (MMIC) amplifiers:

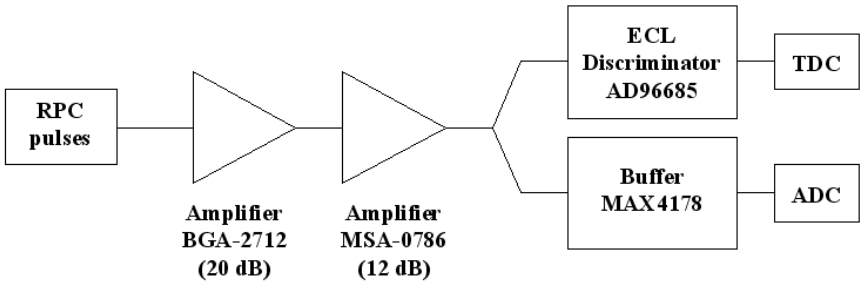


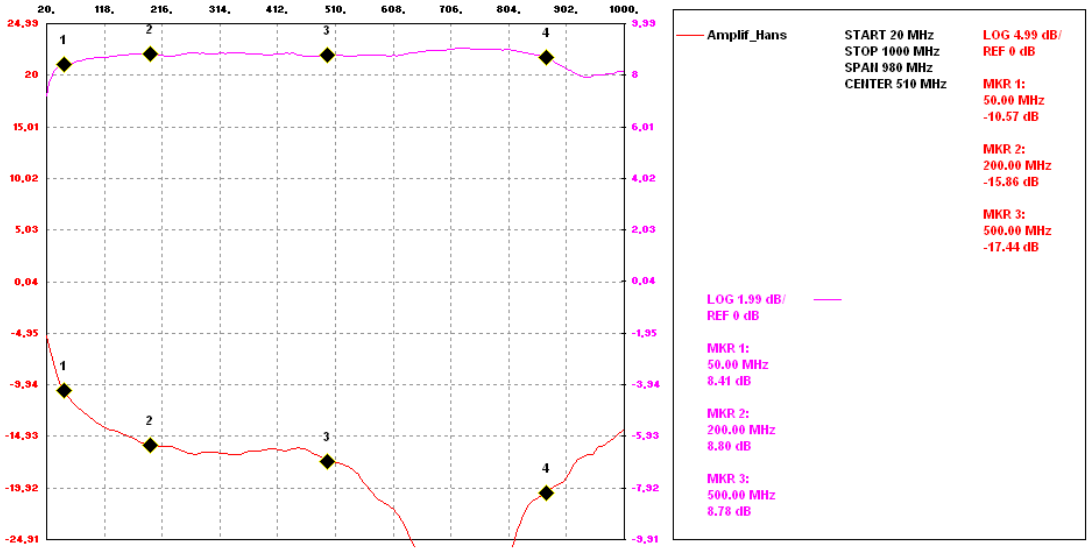
Figure 4.2: *Simplified STEP1 block diagram: i) analog stage with two amplifiers connected to a buffer to measure the charge in an external ADC and ii) digital stage with an ECL discriminator to measure the time information in a TDC.*

- A first preamplifier step (Fig. 4.2) based on the PHILIPS BGA2712, a MMIC amplifier featuring 3.2 GHz bandwidth to 3 dB, a flat gain of 21 dB at 2.6 GHz, a good stability (K>1.5) and good linearity. This means that the preamplifier has a high gain-bandwidth product (GBW>10^{11}).
- A second amplifier step based on an inverter HP Agilent MSA-0786 amplifier, also a bipolar MMIC featuring 2.0 GHz to 3 dB, a flat gain of 12.5 dB at 1 GHz and good stability (K>1) and with a high gain-bandwidth product (GBW>10^{11}).

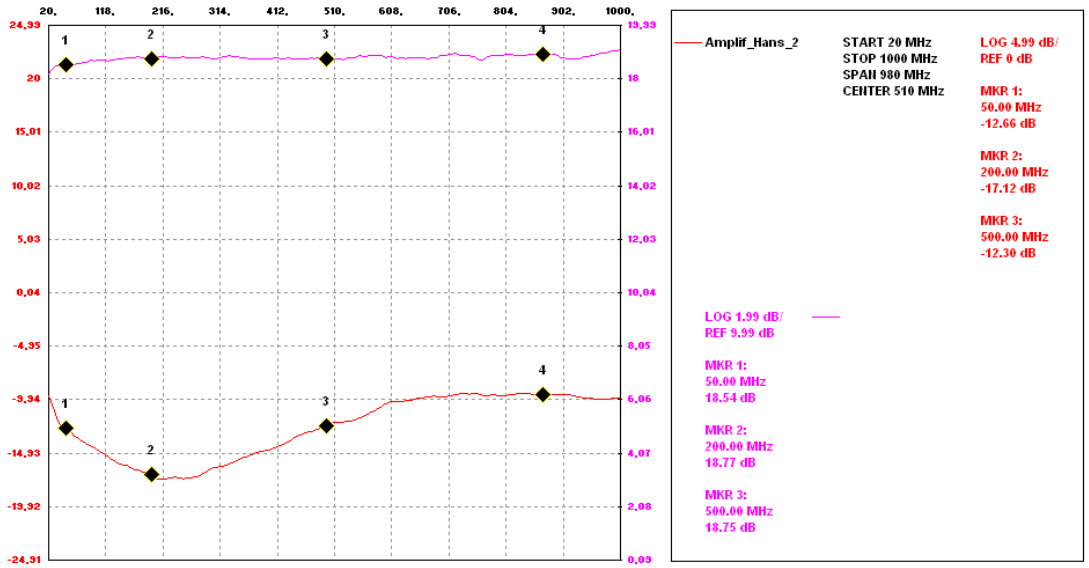
Both amplifiers worked with an input impedance of 50 Ω, which has proven to be quite convenient, allowing the input connection to be made through a standard cable and being sufficiently low to reasonably match the detector impedance [78]. In the design of the board some special technical issues are needed, using the TX-Line program to control the impedance of the paths as function of its width and thickness (specially in the analog part). In this board was easy because there were only two outer layers and not inner layers were used. Other important issues were to connect to ground several points of the board using vias to minimize the parasitic inductances and put coupling capacitors to ground as close as possible to the amplifiers.

Figure 4.3 shows a frequency analysis of the gain of both amplifiers done with a network analyzer and a pulse generator. It represents the gain (in dB) versus the frequency (in MHz). In the case of the BGA2712 (a), the gain was very similar to the theoretical value (∼20 dB) and the difference was inside the tolerances. In the case of the MSA-0786 (b), the gain was lower than the theoretical value because the second amplifier step was saturated in amplitude: for pulse signals bigger than 100 mV at the input of the preamplifier, the MSA-0786 saturated (this did not happen for RPC signals because their amplitudes are smaller).

The output of the second amplifier was split in two branches: (a) one went to the MAX4178 buffer that sends the analog signal to an ADC to measure the charge and (b) the other went to the AD96685 discriminator, where the digital part started.



a)



b)

Figure 4.3: *Frequency analysis of both amplifiers done with a network analyzer and a pulse generator at Televes Company in Santiago de Compostela: MSA-0786 (a) and BGA2712 (b).*

4.2.2 Digital stage

Both amplification steps fed an ultra-fast single ECL discriminator, the Analog Devices AD96685, featuring 2.5 ns propagation delay with 50 ps of dispersion and a low power consumption (118 mW per IC). The discriminator level or threshold was a positive constant level given by a potentiometer. This threshold avoided that the comparator shot again in the noise at the output of the amplifiers. The AD96685

discriminator gave an ECL high level for signals above the threshold. This signal was sent to an external TDC to measure the arriving time of the particles.

After the discriminator stage a digital 3-bit ECL-interface programmable delay line, a Data Delay Devices PDU108H series, was included. The delay line could provide a maximum delay of 280 ns, in steps of 40 ns each. It was needed to guarantee that the signal arrived after the trigger of the TDC. The wanted delay could be selected externally with a switch, that provided a high and a low level at the input of the bits A_0, A_1 y A_2. These bits selected the wanted delay at the output signal. The output of the delay line was sent to the TDC to read the measured time.

The delay line also introduced a problem: the width of the signal at the input of the delay line should be, at least, a 20% of the delay required. This was one of the features of this PDU108H delay line. In order to avoid the problem, a flip/flop was included to freeze the pulse in high state and increasing the time window at two times the required delay. So, the flip/flop was only sensitive to signals having a width twice of the selected delay. The IC we chose for this purpose was the On Semiconductor MC10EL31, an ECL D flip/flop with set and reset functions, featuring 475 ps propagation delay.

4.2.3 Voltage regulators stage

The voltages needed for the board were provided by two voltage regulators, one providing +5 V and the other -5 V. The positive voltage supply was given by the Fairchild Semiconductor LM7805 series 3-terminal regulator through an input voltage of +7 V. These regulators are capable of supplying 2 A of output current.

The negative voltage supply was given by the National Semiconductor LM7905 series 3-terminal regulator through an input voltage of -7 V. This regulators are capable of supplying 1.5 A of output current and they have a high ripple rejection. Both regulators employ internal current limiting safe area protection and thermal shutdown for protection against virtually all overload conditions. The positive voltage was needed for both amplifier steps and for the digital step; the negative voltage was only needed for the digital step.

4.3 FEE-STEP1 performances analysis

In order to characterize the behaviour of the FEE-STEP1 and the whole system RPC and FEE, we developed some different measurements:

- The time resolution σ_T with pulses and real RPC signals.
- The position resolution also for RPC signals.
- The charge of the RPC signals and the possible correlation between the charge and the width of the digital signal through the Time Over Threshold (ToT) to

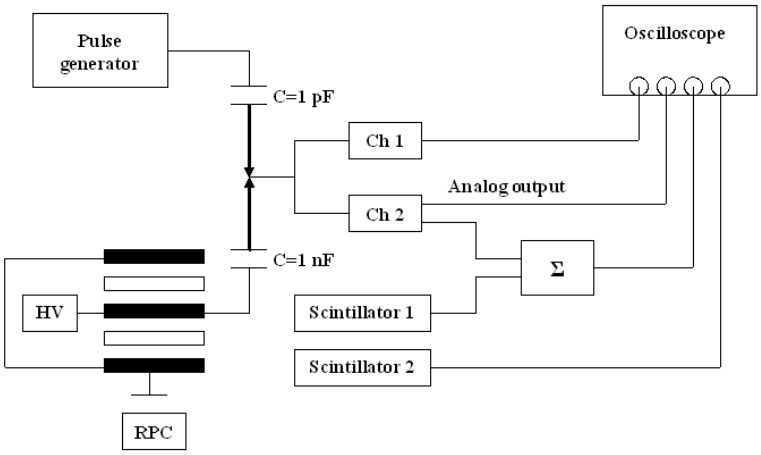


Figure 4.4: *Experimental setup to characterize the FEE-STEP1 and STEP2 with pulse generator (top) and real 4-gap RPC signals (bottom).*

analyze the possibility of implementing the ToT algorithm [79], [80] to measure the charge.

4.3.1 Experimental setup

For the development of this FEE-STEP1 design, the tests explained before were developed both at the LabCAF laboratory at the University of Santiago de Compostela (USC) and at the LIP laboratory in Coimbra for two different cases:

1. With signals coming from a pulse generator through the test input of the FEE.
2. With RPC signals from the first prototype cell used in April 2003 [64], [65].

1. Pulse measurements were performed with pulses from a AGILENT 81130A pulse-pattern generator (two channels; 660 MHz). These external pulses were connected to the test signal input of the FEE channels and the experimental setup is shown in Fig. 4.4. The response of the FEE as an ECL digital output was sent to an oscilloscope, where we measured the time difference between the ECL digital output of the board and the reference signal of the pulse generator. The oscilloscope we used for these measurements was a TEKTRONIX TDS7104, a Digital Phosphor oscilloscope with 1 GHz bandwidth and 10 Gs/s for the four channels. With this method we could measure the time resolution of the FEE as function of the charge injected in the test input. The signals were injected at the test input through a 1 pF capacitor and it could be changed with the pulse generator. Then, the charge through the capacitor could be obtained as follow:

$$V = \frac{q}{C} \longrightarrow q = V \times C \tag{4.1}$$

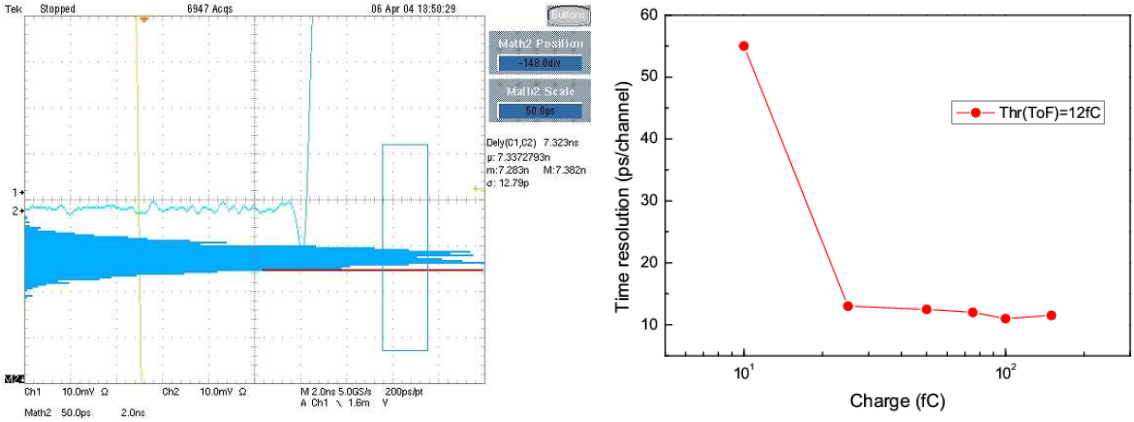


Figure 4.5: *FEE-STEP1 time measurements with test signals: time distribution for one signal input (left), showing a σ_T=13 ps/channel and time resolution for different input charges in log scale (right).*

The amplitude of the pulses changed between 100 mV and 2 V, with a 1 μs width. In the test input, before the C=1 pF, there was a factor 10 voltage divider.

2. The tests done with real RPC signals were more complicated (Fig. 4.4). In this prototype, the standard gas mixture, $C_2H_2F_4$ (85%)+iso-C_4H_{10} (5%)+SF_6 (10%) [38] was used. We used two different FEE channels connected to two RPC cells, doing coincidences between both RPCs and two external scintillators, with a radioactive ^{22}Na between them. This source emits e^+ particles and their annihilation with e^- from the medium produce collinear photons of 0.511 MeV illuminating the RPC. The four signals (two provided by two FEE channels and two by the scintillators) were sent to the oscilloscope. The time difference between both electronic channels was measured using the scintillators as trigger. The width of that distribution gives the time resolution.

4.3.2 Time Resolution analysis

Figure 4.5 shows the FEE-STEP1 time resolution measured with external pulses through the test input. These results correspond only to the electronics contribution. The left side shows an example of the time difference distribution between the output of a STEP1 channel and the reference test signal. The right side shows the time resolution as function of the charge of the input signal, calculated using Equation 4.1. For signals with charges higher than 20 fC, the average time resolution is σ_T=13 ps/channel. The threshold was set to ∼12 fC. For smaller charges (<20 fC), the time resolution get worse to 50 ps/channel. This test was done at the LabCAF-USC laboratory.

The tests done with the whole system, including the RPC, were done at the LIP laboratory at Coimbra. In order to measure the time resolution of the whole chain, RPC+FEE-STEP1+oscilloscope, a HV of 6400 V was applied to the RPC and a

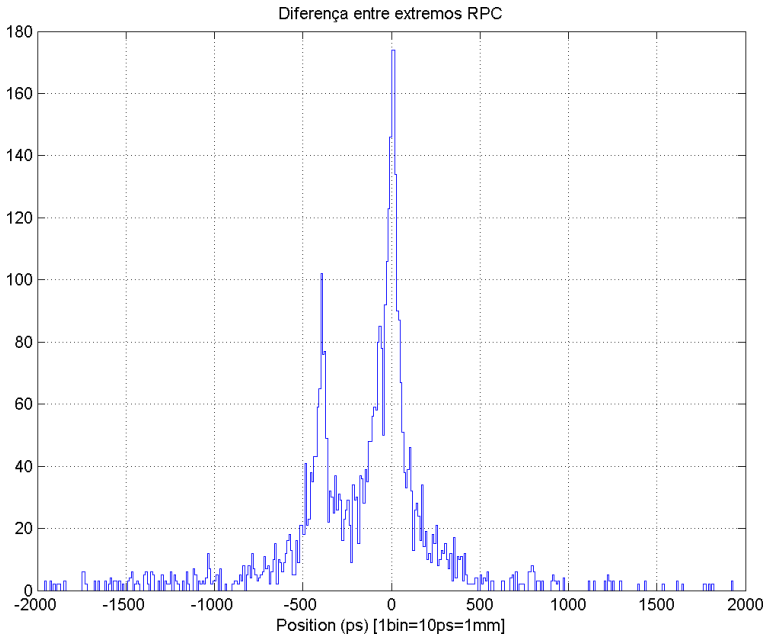


Figure 4.6: *Position resolution analysis of the FEE-STEP1 using two ^{22}Na sources.*

^{22}Na source was used. Two FEE channels were connected to RPC cells. As the ^{22}Na source produces two collinear photons going in opposite directions, two fast scintillators (Bicron BC-420 readout with Hamamatsu H6533 ensembles) were used for triggering the direction and timing of the detected photons.

The time resolution of the whole chain was measured as the width of the gaussian time difference distribution between two STEP1 channels. As the time resolution obtained directly is the combined for two electronic channels, we divided by $\sqrt{2}$ the measured σ_T to obtain the value per channel. The time resolution combined for two channels of the system is 60 ps, giving ∼40 ps per channel. The threshold was set at a minimum value of 10 mV giving adequate immunity with respect to the noise. This result was very successful for the HADES purposes, although it did not include the jitter of the DAQ system because it was measured with a digital oscilloscope.

4.3.3 Position Resolution analysis

Knowing the time resolution of the whole system it is possible to estimate easily the position of an incident particle. For this purpose a good time resolution is needed. The experimental setup was changed, using two ^{22}Na sources placed at a close distance. The position in the cell could be measured through the time difference between both RPC sides using the relation [11]:

$$x = \frac{t_{Left} - t_{Right}}{2} \times v_{prop} \tag{4.2}$$

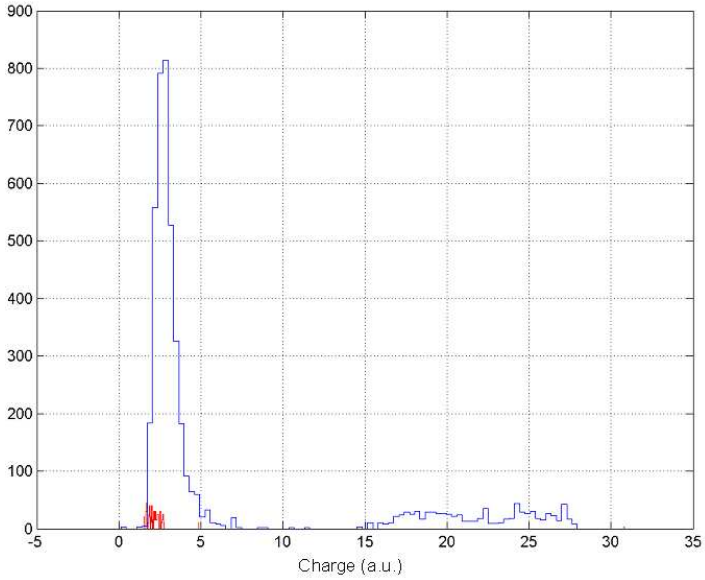


Figure 4.7: *Charge spectrum (a.u.) of the FEE-STEP1, measured with an ADC. Structure at high charges corresponds to streamers and red entries are noise events.*

The signal propagation velocity inside the RPC cell had been previously analyzed, providing a value of $v_{prop} \simeq 2/3$c [22]. Then, the position resolution can be calculated through Eq. 4.3:

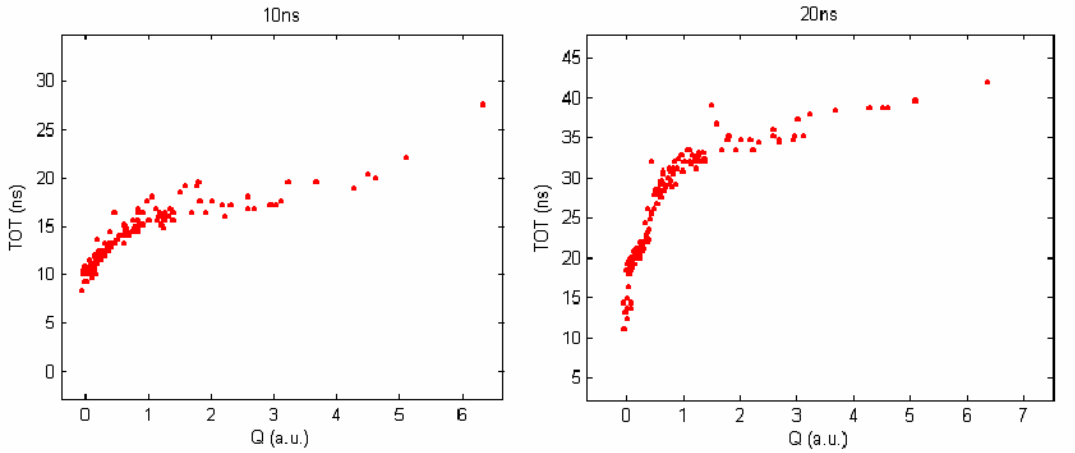
$$\sigma_{pos} \sim \frac{v_{prop}}{2} \times \sigma_T \tag{4.3}$$

where σ_T corresponds to the time resolution measured, that in this case is 60 ps. If this value is replaced in Eq. 4.3, the position resolution integrated over all the positions along the width of the cell is obtained, $\sigma_T \simeq 6$ mm (this is the result of the gaussian adjust of the main peak of Fig. 4.6). This result is in agreement with previous measurements [22], where a position resolution of σ_T=6 mm was obtained with the same RPC prototype.

Figure 4.6 also shows the two peaks corresponding to both ^{22}Na sources. The distance between both peaks corresponds to the distance between both sources, being Δx=4 cm. The width of the main peak corresponds, approximately, to the length of the detector cell, because the RPC was around 60 cm (equivalent to $\simeq$6 ns).

4.3.4 Charge measurements

It is also important to measure the charge of the RPC signals because it is needed for improving the time resolution after correcting the well known time-charge effect ('slewing correction'). In order to measure the charge with the FEE-STEP1 the analog signal (after two amplification steps) was sent to an ADC through the MAX4178 buffer. This setup also allows to monitor those signals for different kind of analysis.



(a) (b)

Figure 4.8: *Q-ToT dependence for the FEE-STEP1, analysis done with MATLAB applying a RC-CR filter of 10 ns (a) and 20 ns (b).*

The charge spectrum of the RPC signals produced with an external ^{22}Na source is shown in Fig. 4.7. This picture shows the pedestal of the charge spectrum, together with a low noise events (red region) in the measurement. The homogeneity of the charge distribution is also shown and a region with higher charges, corresponding to RPC signals with high charges and streamers.

Charge and Time Over Threshold correlation

A possible correlation between the charge of the RPC signals measured with an external ADC an the one measured through a ToT algorithm was analyzed. The goal was to try to implement this method in the next STEP2 design (that method to measure the charge is used by the NINO electronics developed at CERN for the RPCs of ALICE [49], [50]).

Results are presented in Fig. 4.8. The Time Over Threshold (ToT) is an algorithm which allows to send the charge of the RPC signals up to the DAQ electronic codified in the width of the digital output signal. The algorithm consists in integrating the analog signal, doing the width of the digital output proportional to the integrated signal (charge information). The response h provided by a bipolar RC-CR filter was analyzed following Eq. 4.4:

$$h = \frac{\exp -(\frac{t}{\tau})\theta(t) \times (\tau - t)}{\tau} \tag{4.4}$$

comparing it with the results obtaining with the ADC, using the MATLAB. The $\theta(t)$ function is the Heaviside(t) step function. Fig. 4.8 shows the results for two different filter values, 10 and 20 ns. The correlation between charge and width is better for the 20 ns filter because it is more linear for low charges (the most important region

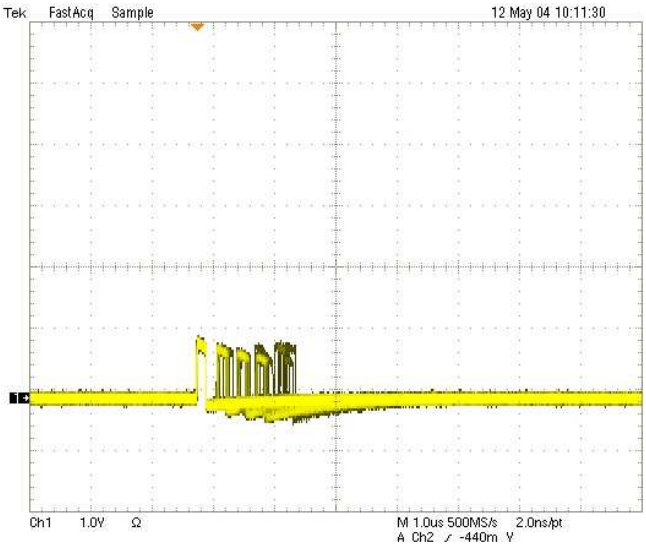


Figure 4.9: *Retriggers at the output of the AD96685 discriminator.*

for the slewing correction) and the width of the ToT changes for a higher range of values, although the slope is very high. Both distributions also show a saturation effect for high charges, corresponding to the streamers produced in the RPC, due to the saturation in amplitude of the preamplifier.

4.4 FEE-STEP1 conclusions

The results presented for the adaptation of the TTL FEE designed by the LIP [78] to ECL logic, the so-called FEE-STEP1, were very promising:

- A time resolution of σ_T=13 ps/channel for the electronics and 40 ps/channel for the whole chain, including RPC and FEE but not the TDC for the acquisition.
- The position resolution and also the charge measurements were also correct.

Some drawbacks observed in this design were the high power consumption (at this stage we did not care about it) and the *retriggers* produced in the AD96685 discriminator (Fig. 4.9). This last effect was due to oscillations in the analog step of the FEE. In the next design, the STEP2, this behaviour was stabilized doing better grounding in the analog part, changing both the discriminator and the delay line for one with a 1 μs constant delay (to avoid this effect during 1 μs after the signal).

The FEE-STEP1 board was used in a research work related with the analysis of the effect the RPC glass temperature facing the improvement of the high rates performances of the detector. Results were very positive and were published in [83].

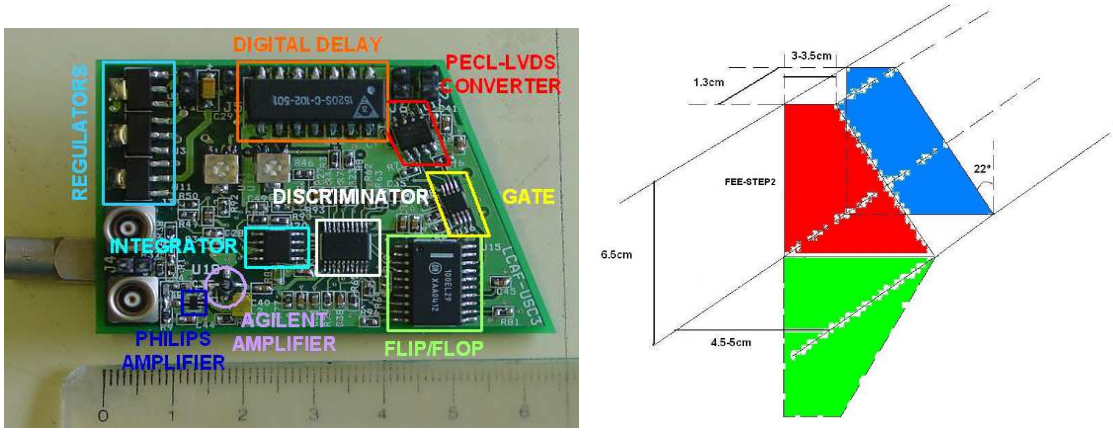


Figure 4.10: *Left: FEE-STEP2 board, with 2 channels in ∼6×4 cm² (∼24 cm²). Right: critical dimensions to fit the STEP2 board in the keep-in volume between RPC detectors.*

4.5 The FEE-STEP2 design

If the FEE-STEP1 was an upgrading to ECL logic of the reference electronic designed by the LIP [78], the next design called FEE-STEP2, also done with ORCAD [81], was not based on the original. The main characteristics were [39], [79]:

- The charge measurement of the RPC signals was implemented through the ToT (Time over Threshold) algorithm, explained in section 4.3.4.
- A time window with a dead-time of ∼1 μs was implemented to avoid *retriggers* of the discriminator (*retriggers* seen in the previous design, Fig. 4.9).
- A single LVDS digital output was used to measure both the time in the leading edge of the signal and the charge through the ToT-width of the signal. This feature means a big advantage because it reduces a factor two the number of channels needed in the acquisition: ADCs are not more necessary and only a TDC channel is enough to deal with both time and charge measurements.

The FEE-STEP2 design [39], [79] was a 2-channel board, with four layers (TOP and BOTTOM for components and two internal layers for ground and power supply planes). A picture of the STEP2 is shown in the left picture of Fig. 4.10, where the new trapezoidal shape of the board is also shown. This new shape was introduced to fit the board in the free available room in the keep-in volume of the RPC detectors (see the right picture of Fig. 4.10). The size of the STEP2 board was ∼6×4 cm², ∼24 cm². In this design, the critical dimension was the 4 cm width which avoids that the PCBs of different RPC sectors crash between them.

As in the case of the STEP1, the design of each channel of the STEP2 could be divided in three different stages:

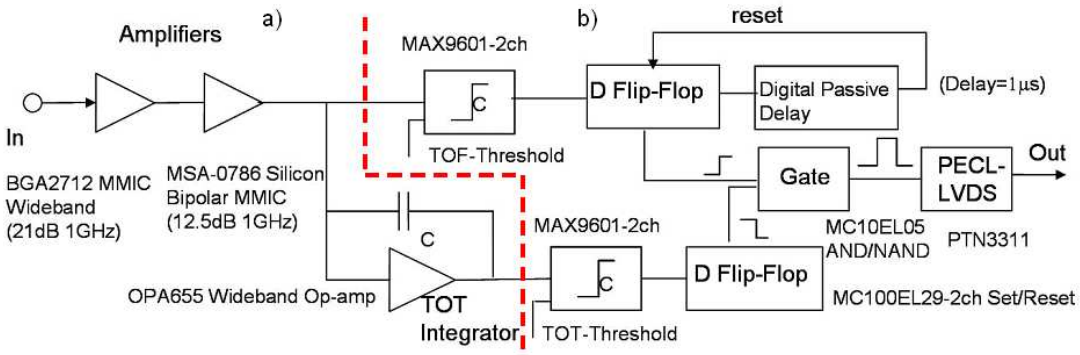


Figure 4.11: *Simplified FEE-STEP2 block diagram: i) an analog part with two amplifiers and another one for the integrated signal to measure the charge through the ToT method and ii) a digital part with an ECL/PECL dual discriminator, a 1 μs delay line to avoid retriggers in the comparator and a PECL-LVDS converter. The LVDS signal was sent to a TDC based data acquisition system (DAQ).*

1. The analog stage with two amplification steps and one amplifier for the integration of the analog signal to measure the charge through the ToT-width.
2. The digital step where time and ToT are codified in a single LVDS signal.
3. The voltage regulation.

The block diagram of the STEP2 design is shown in Fig. 4.11, and the schematic and the layout are given in Appendix A. Other important constraint in the FEE design is the power consumption, that in the case of the STEP2 was 5 W per board (2.5 W/channel) [79], [82]. This was too high in order to avoid the heating of the surrounding detectors. Without taking into account the voltage regulators of the board, the power consumption was reduced to 1.5 W/channel. Let see the main features of each of these three parts.

4.5.1 Analog stage

The analog stage was based in the same amplifiers than in the previous FEE-STEP1 design, a high bandwidth MMIC amplifiers to deal with the very high frequencies (GHz range) expected in the RPC pulses [46], [47]. There were any reason to change them: the amplification was enough, the stability was good and the noise level was reasonable. The gain of both amplifiers shown in Fig. 4.3 as function of the frequency is still valid.

The output of the second amplifier, MSA-0786, was split in two branches: (a) one of them went to the OPA655 Burr-Brown operational amplifier with a big bandwidth which, with an RC circuit (Fig. 4.12), integrates the analog signal to measure the charge of the RPC signal through the ToT algorithm (required for the slewing correction) and (b) the other one went to the discriminator, starting the digital part.

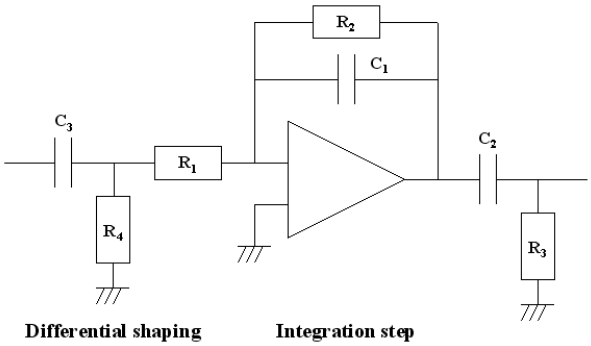


Figure 4.12: *Integration step done with the OPA655 and with two RC's: one to produce a differential shaping first and the second to integrate the resulting signal.*

Figure 4.12 shows the integration step for the RPC pulses: first of all, C_3 and R_4 produce a differential shaping of the analog signal and then, the op-amp integrates the signal, where R_1, R_2 and C_1 give the integration constant and the decay time of the output signal. C_2 and R_3 change the overshoot point of the integrated signal, where the signal comes back to the reference level.

4.5.2 Digital stage

The analog stage was connected to an ultra-fast dual ECL/PECL MAXIM discriminator, MAX9601, with hysteresis, 30 ps of dispersion (lower than the previous one used in STEP1) and a lower propagation delay of 500 ps. It is the same discriminator used in the TACQUILA board for the FOPI experiment at GSI [54] and it is the comparator used in all FEE designs developed since the STEP2, including the final version. Two discrimination constant levels or thresholds were required:

1. A positive level for the time measurements (always higher than 5 mV to avoid *retriggers* in the discriminator due to the noise level at the output of the amplifiers).

2. A negative level for the ToT measurements over the integrated signal. Both thresholds were controlled by a variable resistor.

The design of the FEE-STEP2 was thought for a negative polarity of the RPC signals because positive signals were required at the output of the second amplifier (MSA-0786) and this is an inverter amplifier, as was described before. Then, a positive threshold for the time information was needed. As the integrator OPA655 also is an inverter amplifier (Fig. 4.13-left), a negative constant threshold is needed for the ToT-charge measurements over the integrated signal. The discriminator gives a high PECL level when the output signal of the amplifiers is higher than the threshold, $V_{out}>V_{th}$, providing also a complementary output. The latch enable inputs are fixed, respectively, to a high and low PECL levels with several resistors.

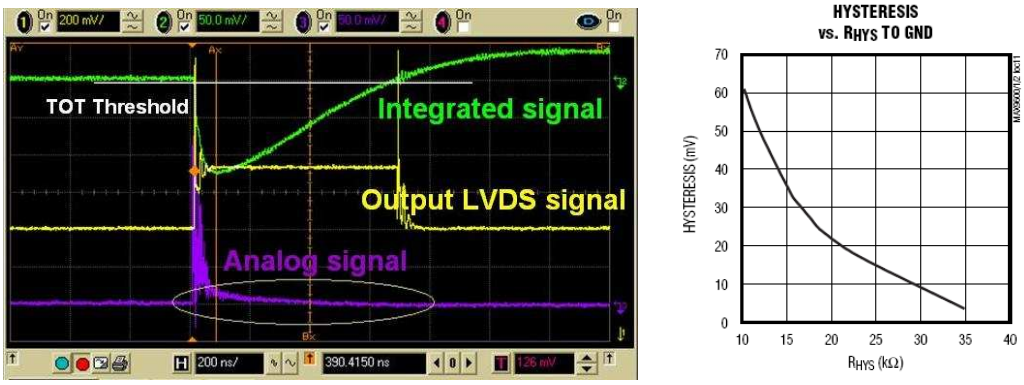


Figure 4.13: *i) Left: RPC signals at different points of the STEP2 board: the output of both amplifiers (violet), the integrated (green) and the LVDS digital (yellow) signals. ii) Right: hysteresis of the MAX9601 discriminator versus the grounding resistor.*

The hysteresis of the discriminator was set to minimum values putting a 33 kΩ resistor to ground at the hysteresis input (Fig. 4.13-right).

After the discriminator step there was an ECL dual differential flip-flop, the On Semiconductor MC100EL29. It is a data and clock D flip-flop with set and reset functions. The idea is, when the leading edge of the ToF signal comes, to frozen it and the pulse is closed when the ToT signal arrives. For this purpose we used a 2-input differential AND/NAND gate to provide the digital output. This gate is the On Semiconductor MC10EL05. Connecting to the flip-flop, a passive delay line of 1 μs was used, the Data Delay Devices Serie-1520. This delay line activated the reset of the flip-flop after 1 μs if any ToT signal close the gate before and rejected any pulse coming during this time (avoiding *retriggers* in the digital signal).

At the end of the digital part, at the output of the gate, there was a high-speed PECL to LVDS translator, the PHILIPS PTN3311. This IC provides a LVDS digital output signal. The LVDS signals [84] are needed to readout the digital signals and a TDC that reads LVDS signals was used. As a robust and immune to noise interface for signal transmission from the MBO to the TRB, the LVDS level logic was chosen. Its low swing and current mode driver outputs create low noise and provide very low power consumption across frequency. LVDS logic levels are smaller (50%) than PECL levels. EMI[3] effects are also reduced, as the signal swings are much smaller than traditional TTL or PECL. These LVDS signals give the time information through its leading edge and the charge information through its width that is proportional to the charge (ToT).

Figure 4.13-left shows an example of the signals produced by a RPC cell at different points of the circuit observed with a high bandwidth scope: (a) the analog signal at the output of both amplifier steps where it shows the ∼1 μs ionic tail

[3]Electromagnetic Interference.

(inside a circle) of the RPC signals, (b) the integrated signal to measure the width-charge information and (c) the LVDS output signal, showing that its width is equal to the width of the integrated signal at the level of the ToT threshold (white line).

4.5.3 Voltage regulators stage

In the case of the FEE-STEP2, three different voltages were needed to feed the board: +5 V, -5 V and +3.3 V. These voltage levels were supplied through three different voltage regulators. All of them were from National Semiconductor.

The LM2940 series 3-terminal regulator supplied +5 V through +7 V at the input and this +5 V voltage was the input of the regulator that supplied +3.3 V, the LM1117. Both regulators had a low dropout current, 1 A and 800 mA respectively, that means a big stability.

The LM337 series adjustable 3-terminal regulator supplied -5 V through -7 V at the input and it has a 1.5 A dropout current. The +3.3 V was only needed for the PECL to LVDS converter in the digital part of the design. All of them have a thermal protection.

4.6 FEE-STEP2 performances analysis

In order to analyze the performances of the STEP2 and the whole chain including the RPC, the following measurements were done at the LabCAF-USC laboratory:

- The time resolution with both test signals and real RPC pulses.
- The charge of the RPC signal through the ToT algorithm [49], [50].
- The crosstalk between channels, measured as the influence of one channel with signal to another one not connected to the RPC.

4.6.1 Time Resolution analysis

Regarding the FEE-STEP2 time resolution tests, as with the STEP1, two kind of measurements were done:

1. With tests signals coming from an external pulse generator through the test input of the FEE.
2. With real RPC signals from the same prototype used in STEP1 tests [64], [65] and with the same standard gas mixture [38].

Measurements using test signals had the same experimental setup than the previous one, except the oscilloscope, that it was an AGILENT 54830B Digital Oscilloscope with a 600 MHz bandwidth and up to 4 Gs/s for 2 channels. The method

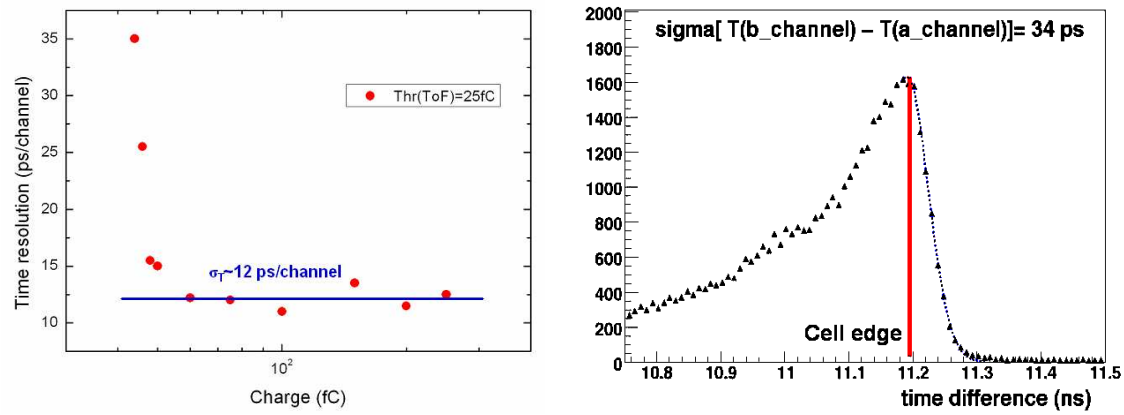


Figure 4.14: *STEP2 time resolution measurements: with a pulse generator as function of the charge (left), giving an average σ_T=12 ps/channel at high charges and with the whole chain RPC+STEP2 (right), measured through the half-Gaussian width at the RPC edge, giving σ_T=35 ps/channel.*

was the same that the one explained in section 4.3.1 and the charge at the input of the electronic channel is calculated with Eq. 4.1. The only difference was that the STEP1 had only one channel with one test input and the STEP2 design had two channels with one test input in each channel, sharing the same input.

Time resolution with test signals

Results for the time resolution of the FEE-STEP2 measured with test signals are shown in Fig. 4.14-left. The average value for signals with charges higher than 50 fC is σ_T~12 ps/channel being worst for lower signals, around 30-40 ps/channel. The ToF and the ToT thresholds were set to 25 fC and -35 mV, respectively.

Time resolution of the whole chain RPC and FEE

The experimental setup shown in Fig. 4.4 is still valid for the time resolution measurements done for the whole chain RPC and FEE-STEP2, although the scintillators were not needed. Both two channels of the board were connected to both ends of the same RPC cell and a ^{60}Co source was used to generate the pulses. This source emits two photons of ~1 MeV not fully collinear. The HV applied to the RPC was changed between 5800 and 6400 V and the work point was set to 6200 V.

The standard way to measure the time resolution with the RPC is through the time difference between the signals at both ends of the same cell when the RPC is exposed to a point-like source. Then, the details in the formation of the pulse cancel at both sides and the only contribution to the time difference is due the jitter of the time measurements. In order to get a good position resolution and to measure a good time resolution, is necessary to focalize the source correctly. But the problem

is that the ^{60}Co source emits two photons not collinear and it is not possible to guarantee a 'point-like' triggering over the cell. A method to overcome this effect is illuminating the cell at one of the edges with the source. If there were no electronic jitter in the time measurements, the time difference distribution between both edges should show sharp-ends at both ends of the RPC. But if there was jitter, the cut becomes smoother taking a gaussian tail shape where the time resolution of the whole system can be measured.

The measured time distribution in timing RPCs is not purely gaussian, being generally visible an excess of events on the longer times (1% or 2%). As can be seen in Fig. 4.14-right, we got a time resolution of 35 ps/channel σ, similar to the STEP1 board. Both tests were done independently using both amplifiers and only the first one to check if a factor of gain $G\sim10$ is enough. In both cases, the results were comparable, showing it was possible to work with only the first amplifier, the BGA2712 ($G\sim10$).

4.6.2 Crosstalk between channels analysis

The presence of the crosstalk between channels in the FEE-STEP2 was analyzed using channels of the same board (worst probable cases). Let's call the channels of the TOP and the BOTTOM layers channels A and B, respectively. The experimental setup consisted on using these two channels, one of them connected to one RPC cell (channel A) and the other one not connected (channel B). The aim was to measure the ratio of the pulses induced in the channel B by the channel A. This test was also done inverting the channels. As this effect depends of the threshold on the discriminator, it was set to a small value, 10 mV. Other important effect that could affect the results was the cabling in the measurements (it was observed that a fan used to control the temperature of the FEE also affected the results).

The most important results for this crosstalk test were:

- The crosstalk in channel A was smaller than a 0.5%. The crosstalk in channel B were negligible.
- There was no explanation about this asymmetry, but the crosstalk is almost negligible. This could be due to the design of the layout of the board.
- Any effect in the time resolution due to fluctuations in the baseline of the signals was observed.

4.6.3 Charge and Time Over Threshold correlation

The correlation between charge and ToT-width of the digital signal was also analyzed for signals provided by a pulse generator and also for RPC signals. As was explained before, the Time Over Threshold (ToT) [49], [50] is a way to measure the charge of the signals integrating the analog signal in such way that the width of

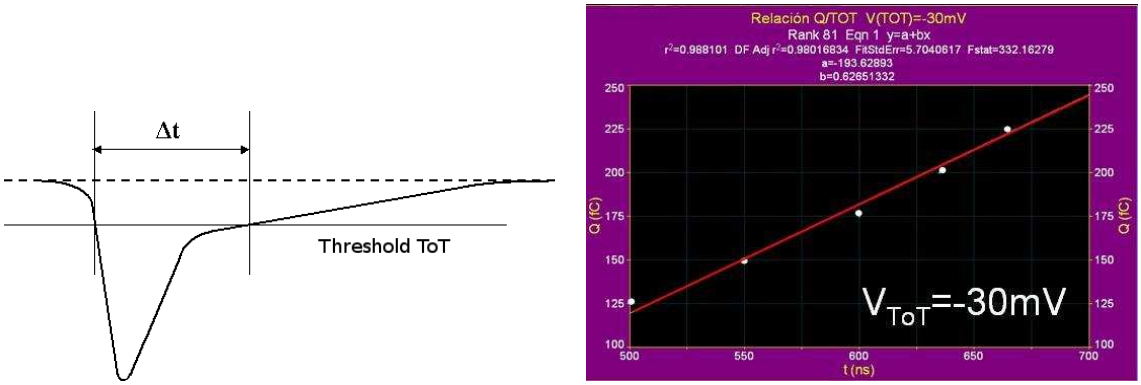


Figure 4.15: *Left: width of the integrated signal, Δt, where it cuts the ToT threshold. The width of the LVDS signal will be equal to this width Δt. Right: relation between amplitude and charge measured through the ToT-width (Δt) of the LVDS signal for pulses coming from a pulse generator.*

the LVDS digital signals is proportional to the charge of the signal. The width of the LVDS output signal Δt is the width of the integrated signal at the level where this signals cut the negative ToT threshold (see Fig. 4.15-left). The upper limit for this width is Δt<1 μs, the value where the reset of the flip/flop is switched on by the delay line if the pulse is not closed before by the ToT signal. The integration constant is giving by the RC and was set to 20 ns.

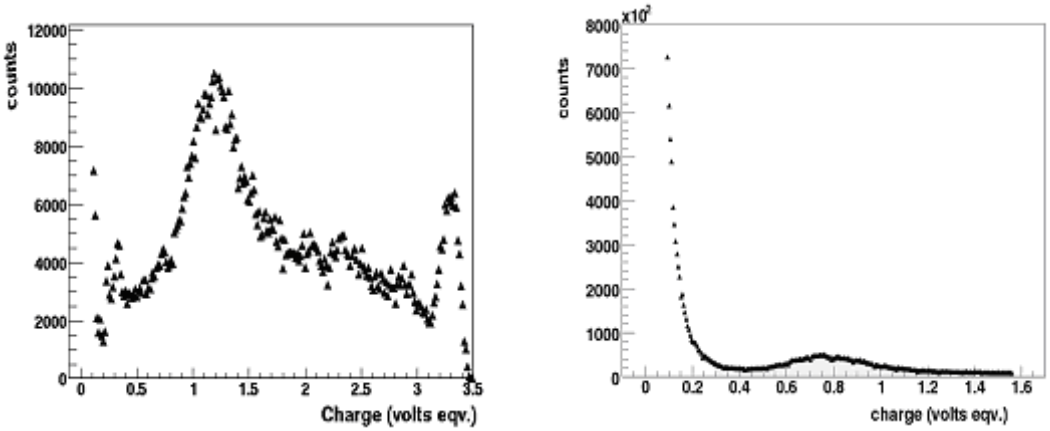
Measurements with a pulse generator

For these tests, the ToF threshold was set to 10 mV, changing the ToT threshold between -10 and -50 mV. For all of these groups of measurements, test signals of different amplitudes (or charges at the input) were used. For each charges the ToT-width of the LVDS pulse output was measured. The ToT threshold level did not work below -10 mV because the integrated signal was very small and the signal was indistinguishable with the noise level.

Figure 4.15-right shows the results for a ToT threshold of -30 mV, showing a good linearity between the ToT-width of the LVDS signal and the charge of the input signals. Furthermore, Δt is smaller for lower charges.

Measurements with RPC signals

Regarding the tests done with real RPC signals, a STEP2 board was used illuminating the RPC with a point-like ^{22}Na source. As it is shown in Fig. 4.13, the width Δt of the LVDS signal is the same that the width of the integrated signal at the level of the ToT threshold. A study with RPC signals were done to see the correlation between the width and the amplitude-charge, through three signals coming from the FEE: the output of both amplifiers, the output of the integration step and the



(a) (b)

Figure 4.16: *Charge spectra for (a) cosmic rays and (b) gamma rays from a ^{60}Co source. The different details of the primary interaction produce quite different spectra. Charge units are the maximum of the integrated signal (V equivalent).*

LVDS digital output (the analog, the integrated and the digital signal in Fig. 4.13, respectively). The response of the ToT algorithm was estimated analyzing the width of the integrated signal at different discrimination levels of the ToT comparator.

In order to define the range of the thresholds needed for this test, the next condition for the efficiencies was used:

$$\varepsilon_{ToF} = \varepsilon_{ToT} \tag{4.5}$$

As efficiencies are related with the threshold values, this condition is equivalent to have, at the same time, a signal in both the ToF and the ToT discriminators.

Previous tests showed that RPC signals for MIPs have an amplitude higher that about 10 mV after two amplification steps with a factor of amplification $G{\sim}40$ [22]. But in those tests there was only one amplifier, the BGA2712, with a gain of 20 dB (a factor $G{\sim}10$). As the gain of the second amplifier (MSA-0786) is 12 dB (corresponding to a factor $G{\sim}4$) we decided to select only amplified signals with an amplitude higher than 10/4=2.5 mV at the output of the BGA2712. Assuming the amplitudes of the integrated signal corresponding to 2.5 mV in the analog signal were $\simeq$15 mV, in absolute value, to obtain charge information for all signals the ToT threshold should be always between 0 and -15 mV. This assumption about the 'minimum avalanche of interest' had to be done because in the laboratory we work with photon sources that shows an exponential enhancement at the lower charges as compared with MIPs (clear peak in charge spectra as expected for ionizing particles, shown in Fig. 4.16).

The left picture of Fig. 4.17 shows a big correlation between the input charge and the charge of the integrated signal. This is the reason why the results presented in

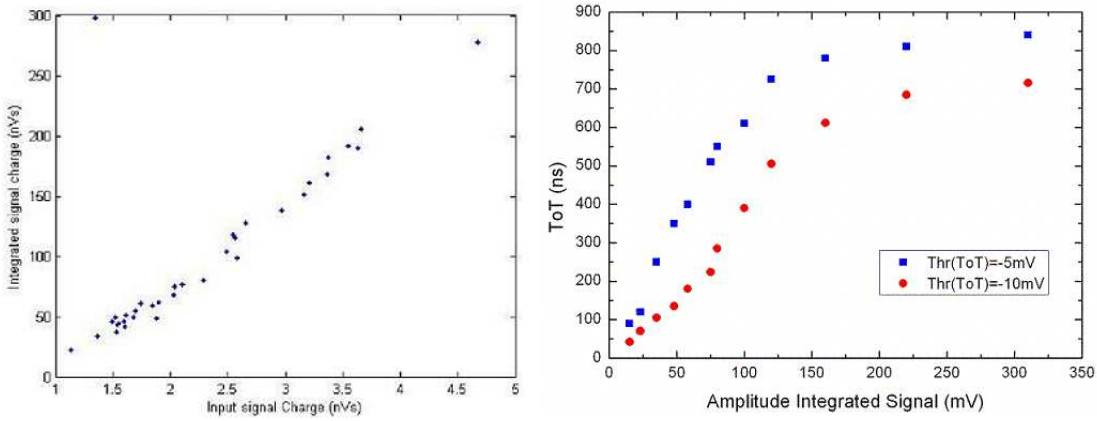


Figure 4.17: *Correlation with RPC signals. Left: between amplitude-charge at the input and for the integrated signal. Right: between amplitude-charge at the output of the integrated signal and the ToT-width of the LVDS signal with two different ToT thresholds, -5 mV and -10 mV.*

Fig. 4.17-right show the correlation between ToT-width and the amplitude of the integrated signal. In this figure the ToF threshold was set to -10 mV and the ToT threshold was set to -5 and -10 mV, respectively.

There are two different regions in the behaviour of the Δt as function of the amplitude of the integrated signal:

1. A first linear region for small and normal avalanches in the integrated signal (A<125 mV).

2. A second saturated region for big avalanches and streamers (A>125 mV).

The explanation for this effect is that for ToT thresholds closer to 0 mV the contribution of the ionic tail of the RPC signals is bigger and also the width of the signal. But in the other way, in the saturation region corresponding to the streamers region, the fluctuations in the measurements were bigger.

In order to solve this problem and taking into account that the most important region for this correlation is the linear region, an analysis with several RC values shown in Fig. 4.12 was done in order to modify the differential shaping, the decay time of the integrated signal and the overshoot point. No differentiator at the input was implemented, and we used it in these measurements trying to suppress the ionic tail of the signals. Results are shown in Fig. 4.18. The thresholds were set to 10 mV for the ToF and -10 mV for the ToT. The RC integration constant was set to 20 ns and the RC_{DIF}, RC_{DES} y RC_{OV} are the differentiation constant, the decay time of the integrated signal and the overshoot, respectively. All these measurements were centered in the linear part of the correlation between charge and ToT.

This plot shows that the best results correspond to the last couple of dates (the pink and the yellow ones). These curves have a differentiation constant of 440 ps, a

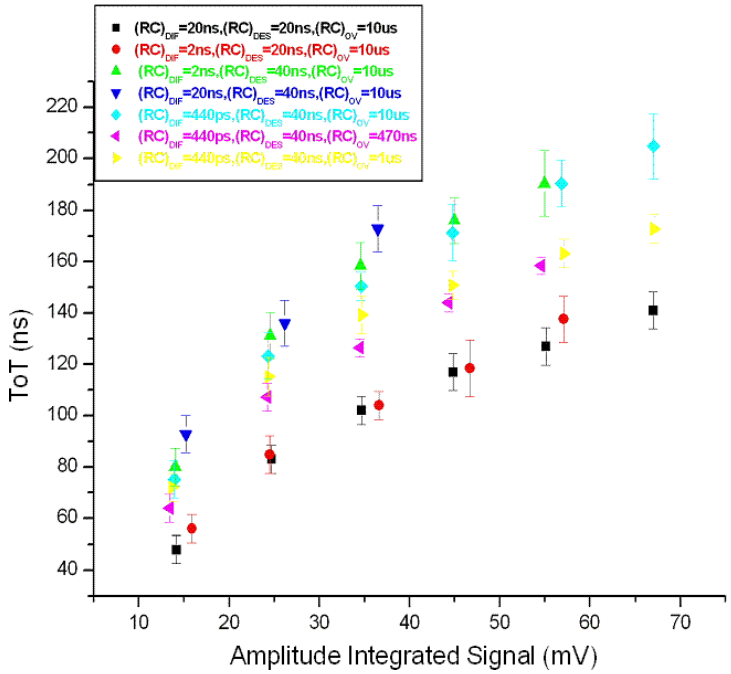


Figure 4.18: *Correlation between amplitude-charge of the integrated signal and the ToT-width of the output LVDS pulse for different RC values with RPC signals.*

decay time of 40 ns and an overshoot of 470 ns and 1 μs, respectively. The behaviour of both curves show a better linearity in the interest region and the error bars of the measurements are smaller. Another characteristic is the higher change in the width of the LVDS digital signal (needed for good measurements in the ToT algorithm).

4.7 FEE-STEP2 conclusions

The FEE-STEP2 design presented in this section show a some good performances:

- A time resolution of σ_T=12 ps/channel for the electronic part and around 40 ps/channel for the whole chain, including RPC and FEE but not the acquisition with the TDC, under illumination with photons of 1 MeV.
- The test show no important crosstalk between channels, less than 0.5%.
- The main feature needed to be optimized was the Q-ToT correlation to measure the charge. Although it was quite linear in the typical avalanches region, it shows a big saturation for big avalanches and streamers. Another point was to investigate if this correlation would be enough for the slewing correction needed for the time resolution measurements.

Even though the good behaviour of the STEP2, the power consumption was still too high. This was not a defect of the design because at this stage of the design

we did not care yet in optimizing the power consumption. Other important feature needed to be optimized was the shape of the FEE board, because the tested shape made very difficult to install the cooling system required to avoid heating effects of the surrounding detectors of the HADES spectrometer.

4.8 FEE first steps conclusions

Two designs presented in this chapter are the first steps developed for the FEE of the HADES RPC wall. Both designs show a good time and position resolutions and a negligible crosstalk between channels. Regarding charge measurements, the STEP1 provided good results but should be measured with an external ADC; STEP2 show promising results but more work was required to improve the ToT algorithm.

An improvement to be introduced in the further steps would be to split the FEE in two separate boards, taking out the voltage regulators to a second board. This is due to the shape of the RPC detectors and room restrictions between sectors being the easiest way to implement the FEE in the final design. For the definitive RPC cells [22] (see chapter 3), the FEE will be divided in two different PCBs [80]:

1. A passive Motherboard (MBO) housing voltage regulators, threshold levels, test signals and also trigger signal shaping needed for the HADES experiment.

2. An active Daughterboard (DBO) with four channels per board instead of the two channels of the STEP2, housing the amplifying and digitizing tasks.

Other important goal for the next steps will be to decrease the power consumption to keep the temperature of the RPC detector in a reasonably low value, as well as the other HADES detector's.

Chapter 5

Simulation of the Front-End Electronics

In this chapter we present the simulations done to optimize the DaughterBOard (DBO) design [82], [80] of the Front-End Electronics of the HADES tRPC wall. The aim of this simulation is to develop the final FEE design, including the changes recommended respect previous designs (STEP1 and STEP2). The simulation of the DBO circuit has been done with the SPICE [85] (Simulation Program for Integrated Circuit Emphasis) tool in ORCAD [81] Corp. of Cadence Design Systems, Inc.

SPICE is a powerful general purpose analog and mixed-mode circuit simulator that is used to verify circuit designs and to predict the circuit behaviour. Computer-aided simulation allows the designed system to be simulated so that the expected circuit behaviour can be verified under specific operating conditions, any design errors can be identified and the system performance can be refined by fine-tuning relevant parts of the design. Hence, costly mistakes can be avoided well before the final hardware implementation of the circuit. This is very important for integrated circuits. SPICE was originally developed at the Electronics Research Laboratory of the University of California, Berkeley (1975). PSPICE is a PC version of SPICE (which is currently available from ORCAD). SPICE is a general-purpose circuit program that can perform analysis on various aspects of electronic circuits: the operating point of transistors, time and frequency domains response, effects of parameter variations, Monte Carlo analysis...

The simulation process is divided into three main parts:

1. Drawing the circuit diagram using a schematics software, called Capture from ORCAD. Capture is a user-friendly program that allows to capture the schematic of the circuits and to specify the type of simulation (time, frequency, etc.).

2. Setting up the simulation parameters for the type of analysis selected and running the simulation itself.

3. Observation/evaluation of simulation results for different parameters.

In addition, PSPICE has analog and digital libraries of many standard components (such as NAND, NOR, flip-flops, MUXes, FPGAs, PLDs and many more digital components) which simulates the behaviour of the IC. This makes it a useful tool for a wide range of analog and digital applications. All the passive components (resistances, capacitors and inductances) are included in the analog PSPICE library. All these analysis can be also done at different temperatures to study this effect over the components. The default temperature is 300 K (27 °C).

5.1 DBO-STEP3 simulation for positive signals

The new version of the FEE was simulated for positive pulses at the output of the preamplifier. With this simulation we tried to avoid the possible important mistakes in the circuit design, but this does not mean that the simulation results and the real circuit behaviour would be the same. A correct work in the simulation is a required condition but it is not enough for the good behaviour of the final design. The reason is because all the electronic effects in a real circuit are not included in the simulation and the models of the components are only approximations of the real IC.

5.1.1 DBO-STEP3 simulation circuit description

The electronic design implemented for the DBO board simulation is shown in Fig. 5.1. The MBO is not included because it is a passive board which provides the power supply to the DBO and distributes thresholds and test signals. The schematic is divided in three steps, corresponding to the three important signals needed:

- The first step corresponds to the analog stage, with the amplifiers BGA2712 and MSA-0786 connected in cascade. Both components were not included in the simulation because its SPICE model were not available. This step was also tested in the same configuration in the previous design. Then, we supposed an ideal response, being the signal proportional to the detector signal and the proportionality constant is the amplification factor of both amplifiers.

- The second step is the integrated stage, done with the OPA655 op-amp SPICE model, similar to the one used in the real version (the TI OPA690). In this step the amplified analog signal is integrated. This integrated signal goes to the dual discriminator to obtain the digital PECL signal necessary to measure the charge of the signal deposited for the particle in the RPC, through the Time over Threshold (ToT) algorithm [49], [50], [39].

- The last step is the digital stage, done with the SPICE library of the MAX9601 discriminator (the same than in the real version) to digitize the analog signal. In the DBO design, this signal is converted to LVDS and sent to the MBO and its leading edge gives us the time information. This conversion was not included in the simulation because it is not relevant for the results.

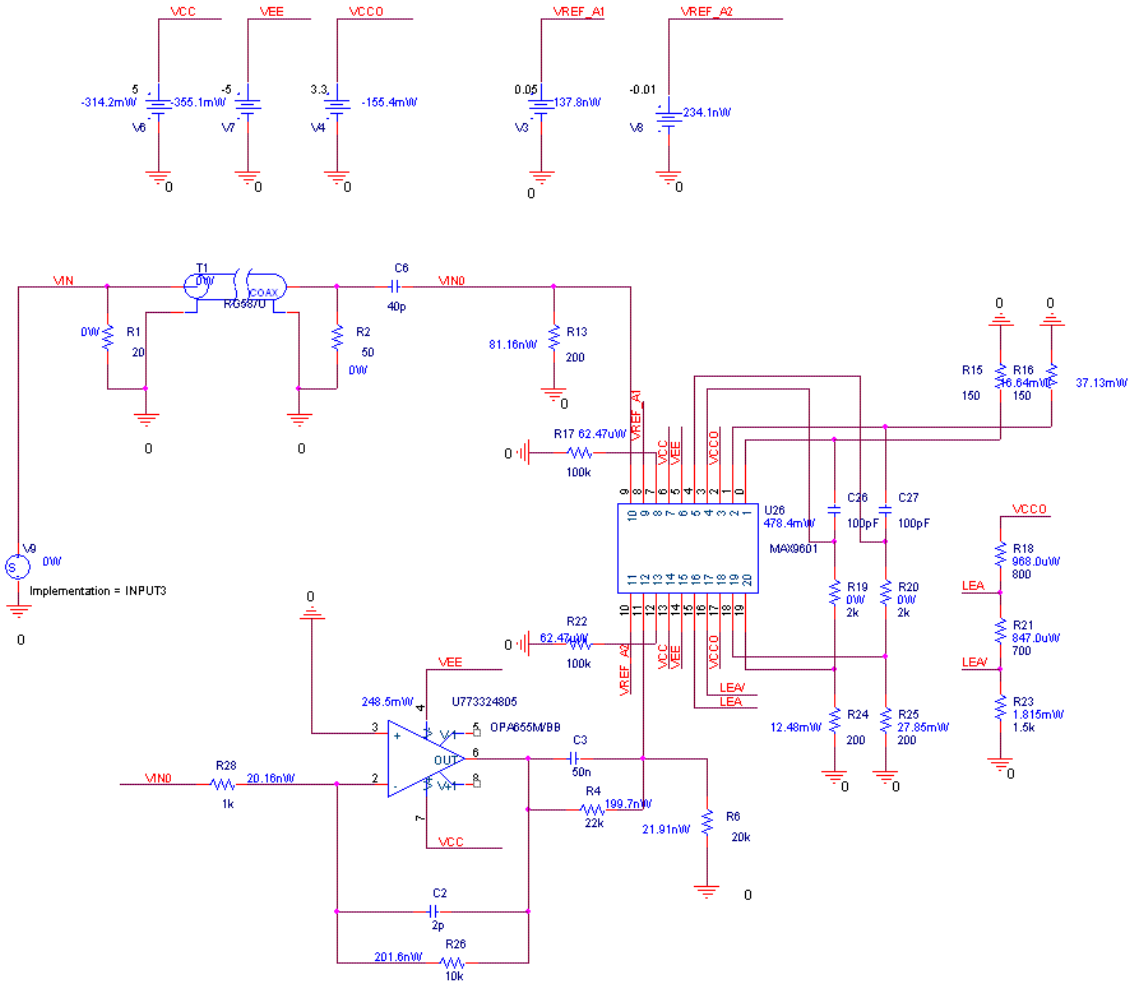


Figure 5.1: *DBO-STEP3 schematic design used in the PSPICE simulation.*

5.1.2 DBO-STEP3 simulation results

The PSPICE simulation was done mainly to improve the active part of the FEE, the so-called DaughterBOard (DBO). The simulation was focused in the analog and in the digital stages, before the PECL to LVDS conversion done at the DBO level. Finally, this LVDS signal of each channel is sent to the acquisition board through the MotherBOard.

Analog stage

Figure 5.2 shows the input signal used in the simulation (red signal), which has two different parts: a fast ∼1 ns pulse simulating the electronic contribution to the detector response and a slow 1 μs pulse simulating the ionic tail of the signal [19]. For the simulation, the amplitude was set to 800 mV.

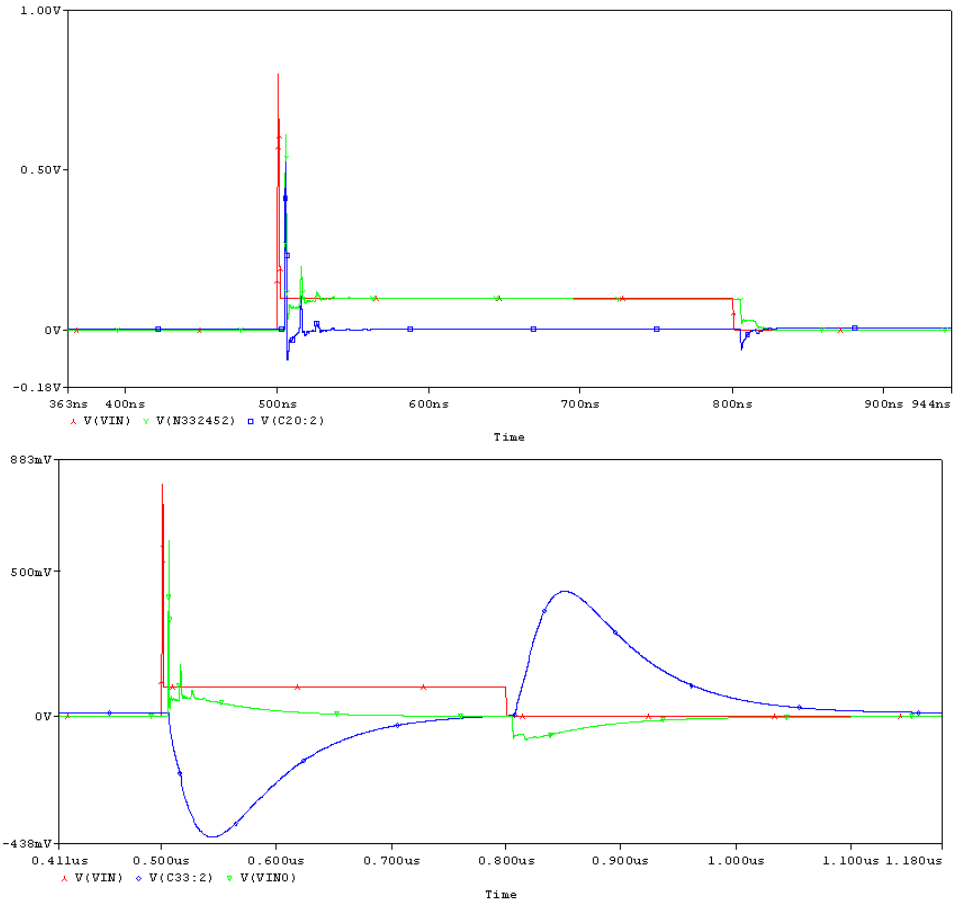


Figure 5.2: *Analog signals of the DBO-STEP3 simulation. The upper plot shows the output of the cell (red), the input of the DBO (green) and the output of the amplifier (blue). The lower plot also shows the output of the integrator (blue).*

The RPC detector is simulated over the input signal through a mismatch transmission line with 20 Ω of characteristic impedance in the detector part and 50 Ω at the electronic input (see the transmission line T_1 in Fig. 5.1). The effect in the input signal is shown in the green signal. The upper picture of Fig. 5.2 shows the input of the ToF discriminator (blue signal) through the input capacitor and resistor, C_6 and R_{13}, where the ionic tail of the input signal disappears due to the differentiation done through this RC. The lower plot of Fig. 5.2 also shows the output of the integrator or the input of the ToT discriminator. The red signal is the input, the green one is the input of the integrator and the blue one is the input of the ToT discriminator. The integration constant is given by R_6 and C_3. After this pulse an overshoot is produced and the total charge integrated is 0. This is not a problem although, if there is a pulse immediately after, a pile-up effect could appear (see Fig. 5.4). This effect was avoided in the STEP2 design with the digital delay line.

Digital stage

After the analog part, the simulation design is split in two different branches to obtain the other two important signals, the digital and the integrated ones:

- One of them goes directly to a dual Maxim MAX9601 discriminator (the same we used in previous STEP2). This is a dual ECL/PECL discriminator, featuring 500 ps propagation delay and ultra-high speed comparator. We need one of these dual MAX9601 for a single RPC-signal, one channel for the ToF and another channel for the ToT discriminator.

- The second one goes to the Burr-Brown OPA555 for the integrated step, a wide-band unity gain stable voltage-feedback operational amplifier. This is needed for the charge measurements through the Time Over Threshold (ToT) algorithm [49], [50], [39]. The output of the integrator goes to the same dual discriminator to produce a digital signal proportional to the charge.

Results for the digital signals are shown in detail in Fig. 5.3, where the different contributions to the total width of the digital signal are presented. The upper picture shows the Latch Enable (LE) signals for the ToF discriminator (the LE is the green signal and the $\overline{LE}$ is the red one). In the lower picture the outputs of the ToF discriminator (blue signal) and the ToT discriminator (orange one) are also shown. The outputs of both discriminators are connected by a combination of capacitors and resistors (R_{19}, C_{26}, R_{20} and C_{27}) and these combinations are connected to both Latch Enable signals of the ToF discriminator (the Q output connected to the LE and the $\overline{Q}$ to the $\overline{LE}$, respectively). For the ToT discriminator, the Latch Enable signals are connected to two different fixed voltage levels.

When the input signal of the discriminator cuts the threshold level (in the simulation threshold$_{ToF}$=50 mV) the output of the ToF discriminator changes the level, and the output signal starts. Immediately, the Latch Enable signals of the discriminator change their levels, freezing the pulse level during a minimum time giving by the discharge time of the combination of R_{19}, C_{26}, R_{20} and C_{27}. When the ToT discriminator shoots, the discharge of the RC stops until the output of the ToT comparator close the signal, starting again the discharge (Fig. 5.3). The discharge time is given by the condition that both Latch Enable voltages are the same. When this happens, the ToF discriminator comes back to the discrimination mode and the output signal is finished. This condition can be written mathematically as:

$$Ae^{-t/RC} = A(1 - e^{-t/RC}) \tag{5.1}$$

The solution of this equation is:

$$2Ae^{-t/RC} = A \Rightarrow \frac{-t}{RC} = ln(0.5) \Rightarrow t = 0.693(RC) \tag{5.2}$$

where for this simulation R_{19}=R_{20}=1 kΩ and C_{26}=C_{27}=100 pF. Then, from a theoretical point of view, t$\approx$70 ns, as it is shown in Fig. 5.3. But in the real life the equal

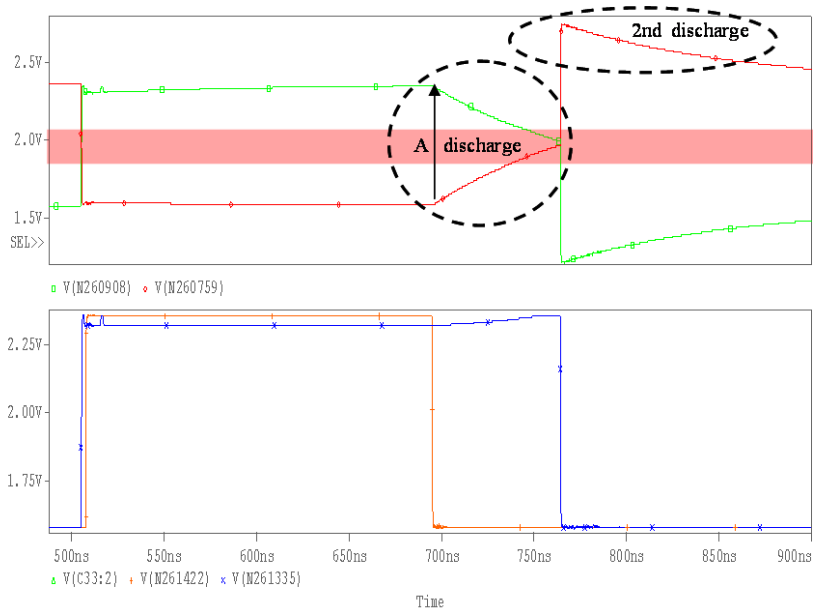


Figure 5.3: *Up: LE (green) and $\overline{LE}$ (red) signals for the ToF discriminator, showing the red region corresponding to the indetermination in the cross point of both LE signals (Eq. 5.3). Down: output of the ToF (blue) and the ToT discriminator (orange), all for the DBO-STEP3 simulation.*

condition given by Eq. 5.2 is not completely true and looking at the discriminator data sheet the transition is produced whenever:

$$|Ae^{-t/RC} - A(1 - e^{-t/RC})| = |A(2e^{-t/RC} - 1)| < 250\ mV \tag{5.3}$$

This condition is represented by the red band in Fig. 5.3. This indetermination does not affect the leading edge of the digital pulse giving the start time information (ToF) but it affects to the width of the pulse which gives the charge information (ToT). This effect could be avoided replacing the RC combination by a flip-flop at the output of the ToT discriminator as we did in the previous design. At the same time, at the end of the digital pulse a second discharge is produced again which even without affecting the the pulse itself it could produce a pile-up effect in the following pulses (Fig. 5.4 shows the electronic response to two identical pulses separated 200 ns). The width of the digital response to both pulses should be identical but the pile-up effect shortens the width of the second output (this effect could be avoided connecting the RC paths to two fixed voltages of 1.6 V and 2.4 V instead of to the outputs of the ToT discriminator, but it would produce an increase in the number of components).

We could also obtain the time t_1 needed in order that the time difference between two consecutive pulses be shorter than a certain value (Δt) for a given RC combination as:

$$t_1 > -RC \ln(\frac{\Delta t}{RC}) \tag{5.4}$$

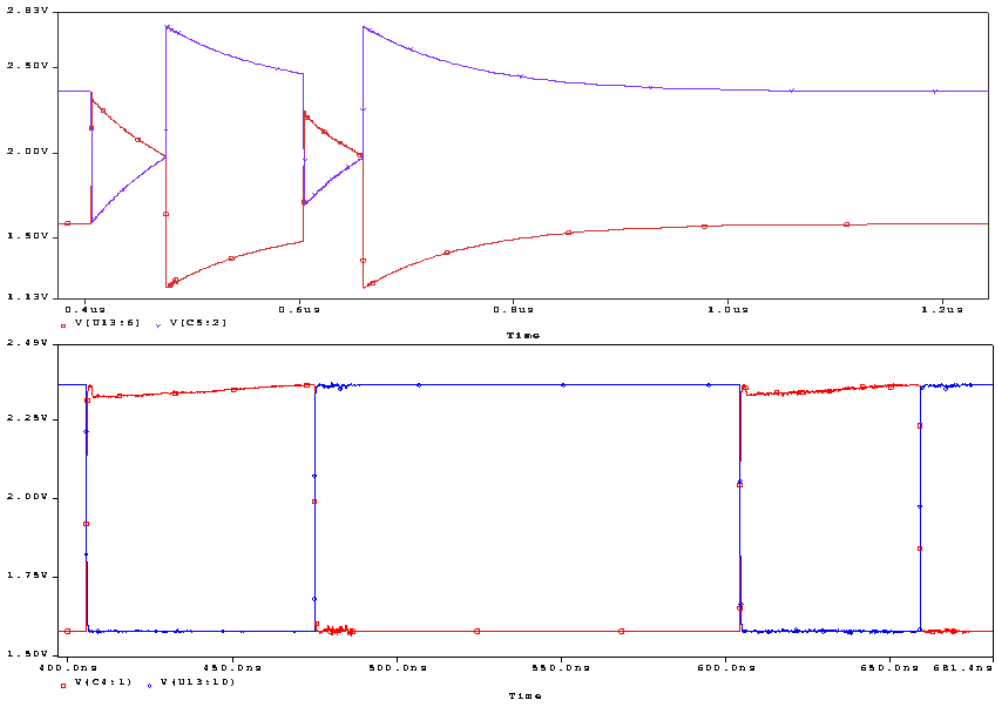


Figure 5.4: *Up: pile-up effect in the latch enable signals. Down: discriminator response to the pile-up effect, both for the DBO-STEP3 simulation.*

Time Over Threshold correlation

The last item done concerned with the simulation of the DBO-STEP3 was to analyze the behaviour of the ToT-width of the digital signal as function of the charge of the signals for different amplitudes of the input pulses of the circuit.

Results are presented in Fig. 5.5, showing two different behaviours for this curve: i) a first region for small signals where the behaviour is linear (for amplitude pulses smaller than 125 mV and ToT<135 ns), and ii) a second region for bigger signals where the ToT saturates (for amplitudes pulses higher than 125 mV and ToT>135 ns). The minimum width for the digital signals is ∼70 ns, being the maximum ToT range <200 ns. The saturation effect in the simulation is due to the amplitude saturation of the op-amp which is working as integrator. This effect must be analyzed carefully because a very good correlation between the width of the digital signal and the charge of the RPC pulses is required.

5.2 DBO-STEP5 simulation for negative signals

Once we have decided to go to a FEE design including only one preamplifying step and we have chosen the BGM1013 preamplifier from Philips (having a high range for negative signals which could help to obtain a big linear region for the ToT curve), a simulation for negative pulses at the output of the preamplifier was done.

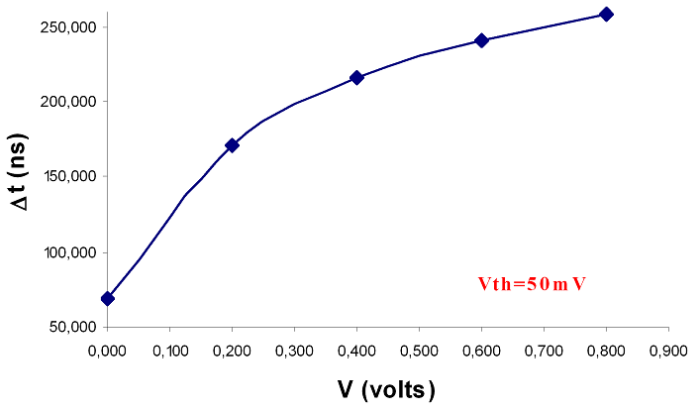


Figure 5.5: *Time over Threshold analysis: width of the digital signal versus the amplitude of the input signal, done with the simulated circuit.*

5.2.1 DBO-STEP5 simulation circuit description

The electronic design implemented for this simulation is shown in Figure 5.6, corresponding only to the active DBO (not included the MBO either). The schematic is divided in three different steps, corresponding to the three important signals needed:

- The first step is the analog stage, with a general amplifier of one SPICE library. It is not the BGM1013 used in the real boards. But that model is equivalent to the BGM1013, being a voltage amplifier. With this model the gain of the amplifier can be changed externally (the original BGM1013 has 35.5 dB gain).
- The second step is the integrated stage, simulated with the OPA690 op-amp SPICE model, the same than in the real circuit. In this step the output of the amplifier is integrated in order to measure the charge of the signal, through the width of the digital signal ('QtoW algorithm') [56].
- The last step is the digital stage. It consists in a discriminator, using the SPICE library of the MAX9601 (the same than in the real circuit), to digitize the analog signal. This signal is converted to LVDS in the DaughterBOard (DBO), before it is sent to the MotherBOard (MBO). But we avoid this last step in the simulation because it is just a conversion with a PECL to LVDS receiver.

This circuit used in the SPICE simulation is similar to the real design for the HADES-RPC electronics. The RPC detector is simulated implementing two 16.3 Ω impedance lines (the real cells have 20 Ω impedance), done with a combination of resistors, capacitors and inductances (Fig. 5.6). These impedance lines produce a delay of 2 ns each and they generate an exponential rise of the signal, deteriorating the rise time somewhat.

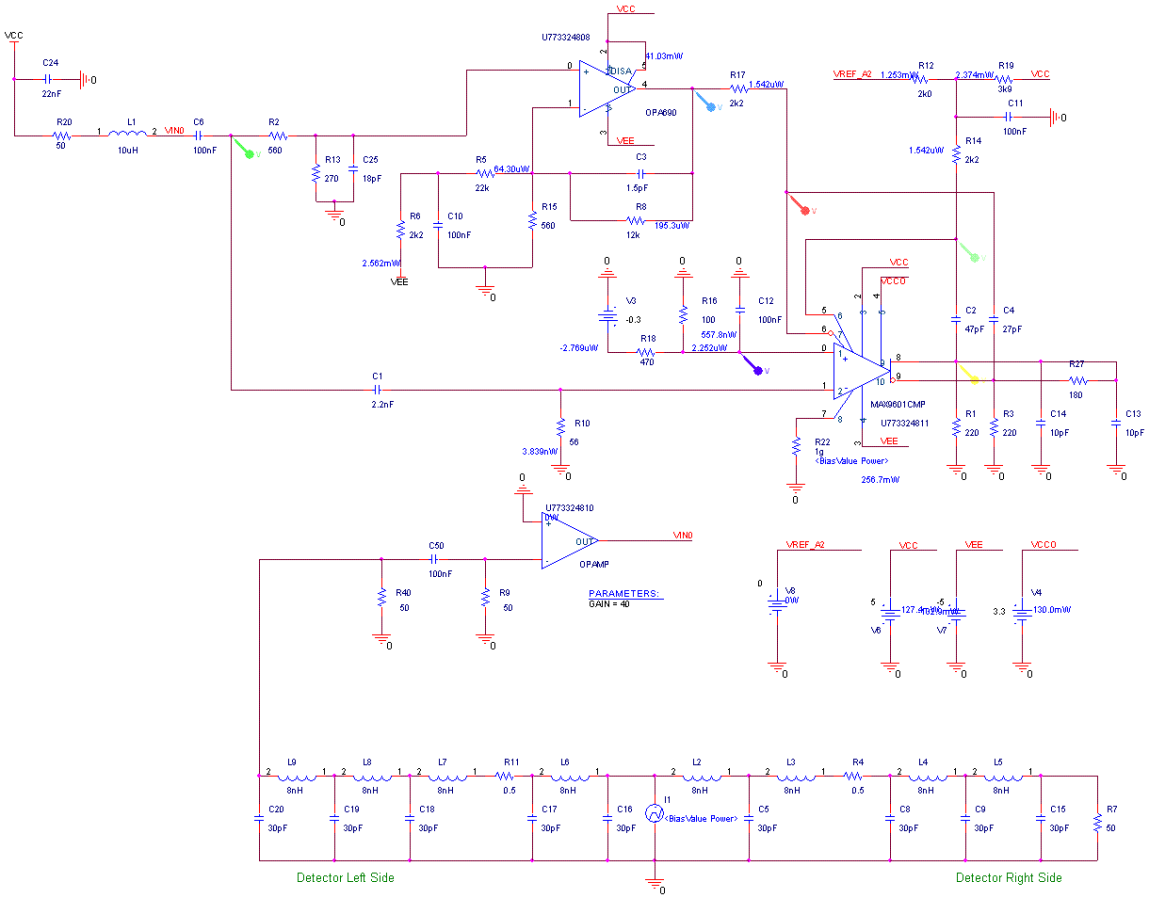


Figure 5.6: *DBO-STEP5 schematic design used in the simulation, showing the simulation of the RPC cells in the lower part and the analog and the digital stages.*

5.2.2 DBO-STEP5 simulation results

The PSPICE simulation was focused on the analog and the digital parts, before the PECL to LVDS conversion done at the DBO level.

Analog stage

The simulation was done using a general PSPICE voltage amplifier instead the original Philips BGM1013 used in the real design. With this amplifier, the response of this circuit for different amplifier gains was calculated: the BGM1013 has 35.5 dB power gain at 1 GHz (a factor $G{\sim}40$ of gain). The study was done for different gains of the amplifier between 40 and 200: 50, 100, 150 and 200 (see Fig. 5.7-left). It was done changing the voltage of the input signal. These results correspond to coupling capacitors of 100 nF at the input and at the output of the preamplifier. If we decrease these capacitors, there is not significant change in the current in the analog part. The only difference is that the positive undershoot of the analog signal is

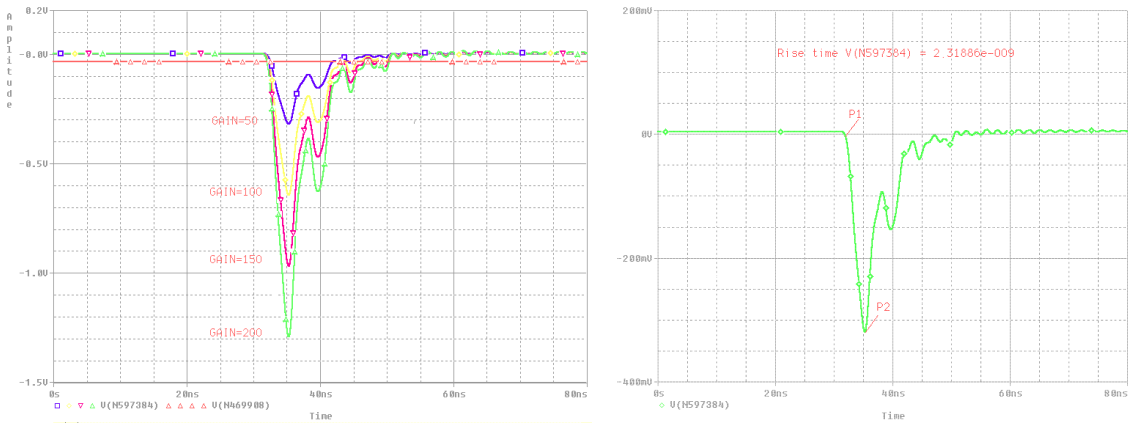


Figure 5.7: *Left: simulated analog signals for different gains; the threshold level is also shown. Right: rise time of the analog signals in the DBO-STEP5 simulation.*

bigger when these coupling capacitors are smaller. Then the width of the digital becomes shorter because the amplitude of the integrated signal is smaller and its undershoot is also bigger.

Fig. 5.7-right shows the rise time of the amplified output signal. The rise time is around 2 ns, similar to the rise time of a typical fast RPC signal. In this way we can simulate the response of the circuit to signals similar to RPC signals (rise time and also rebounds due to the impedance mismatch between the cells and the FEE) in an easy way.

Figure 5.8 shows the Fourier analysis done for the analog signals generated at different amplitudes. The continuous Fourier transform is one of the specific forms of the Fourier analysis. It transforms one function into another, which is called the frequency domain representation of the original function (where the original function is often a function in the time domain). In this specific case, both domains are continuous and unbounded. So, this picture shows the frequency spectrum of the original signals, corresponding to the harmonic analysis of these signals. Figure shows that in the signals dominate the frequencies below 300 MHz, although there are some peaks around 400 MHz and 600 MHz.

Digital stage

After the analog part of the circuit, the simulation is also split in two different branches (as previous version) to analyze the other two important signals:

- One branch goes to the Texas Instrument (TI) OPA690, a wide-band voltage-feedback operational amplifier performing the integration for the charge measurements through the 'Charge to Width' (QtoW) algorithm [56], equivalent to the ToT implemented in the previous version. Now the output of the integrator is connected to the $\overline{LE}$, being the width of the digital output proportional to the charge. With this configuration, we only need one discriminator for

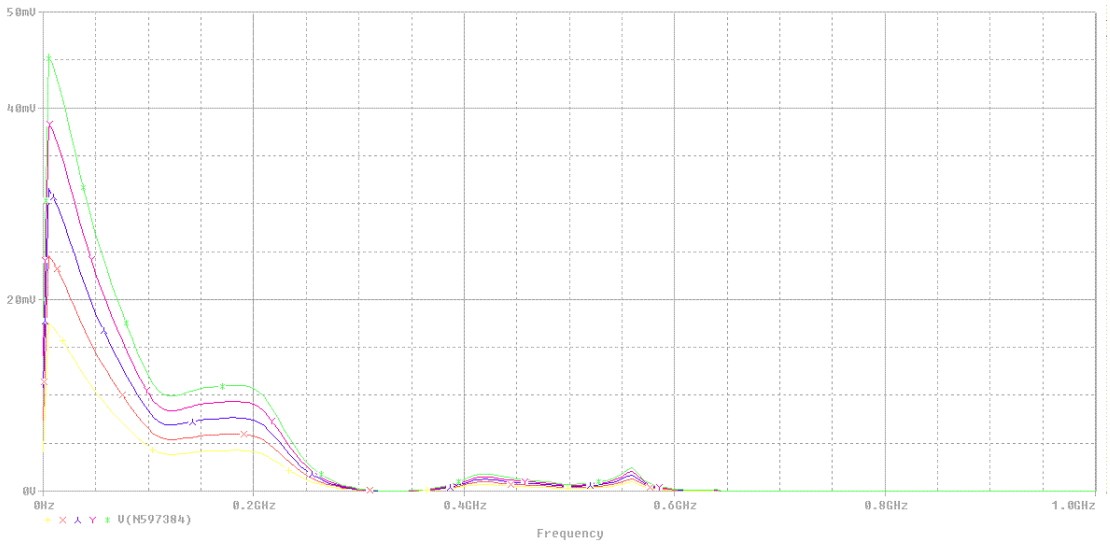


Figure 5.8: *Fourier analysis for different gain values of the analog signals, being dominated by the frequencies below 300 MHz.*

the time measurements, being not necessary for the charge (see chapter 6 for details). At the input of the op-amp a capacitor of 18 pF to ground was introduced to stabilize the op-amp and to avoid high frequency oscillations.

- The other branch goes to the digital step, a Maxim MAX9601 discriminator. This is the same dual ECL/PECL discriminator used in the previous simulation. One of these discriminators are needed every pair of channels, only for the ToF comparators (instead of one per channel needed in the previous design, due to the QtoW algorithm). The previous 18 pF capacitor also reduces the feedback from the discriminator output to the input.

In this simulation the libraries correspond to the same both components that we use in the real DBO design. Results for a factor gain $G{\sim}100$ are presented in Fig. 5.9-left, showing all important signals for this electronic design. The lower part of this figure shows the analog signal, corresponding to the output of the amplifier (blue signal) and the integrated signal (the yellow one). The upper part shows the digital signals: the discriminator builds the leading of the PECL output (blue signal) through a constant threshold (-30 mV in this case), and the Latch Enable signals (LE is the red signal and $\overline{LE}$ is the green one) provide the trailing edge of the digital signal when both signals cross through.

The $\overline{LE}$ is connected to the integrated signal to measure the charge signal through the QtoW method and the LE to an external DC level to control the output width changing its baseline. In this way, the digital pulse encodes both the timing and the charge of the signals. The red and the blue signals show a small rectangular distortion that indicates the region where the discriminator input fires. But due to the enabled Latch, this has no impact on the output signal. Figure 5.9-right

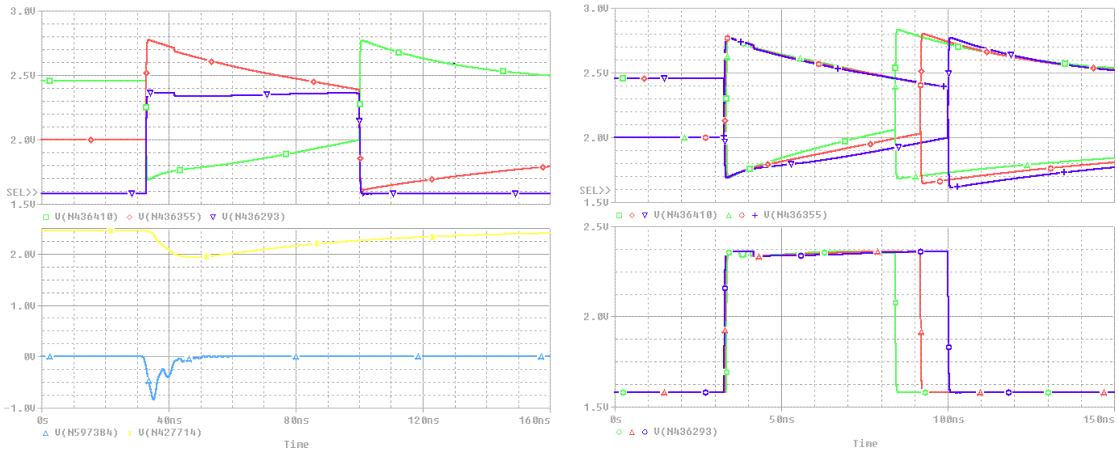


Figure 5.9: *Left: simulation of the digital step for a factor 100 gain, showing all significative signals: i) in the lower part, the blue and the yellow ones correspond to the analog and the integrated signals, respectively and ii) in the upper part, the red and the green signals correspond to the LE and* $\overline{LE}$*, respectively, and the blue one is the output of the discriminator. Right: simulation response to different gains, showing the discriminator output and the LE and* $\overline{LE}$ *signals.*

shows the response of the design simulation for different gains, equivalent to different amplitudes. Only the digital signals are shown in this picture, where lower signals are the output of the discriminator and the upper signals are the LE and $\overline{LE}$ signals.

Figure 5.10 shows, with more detail, the results for the digital response of the design for more gain values between 50 and 150. Only the discriminator output and the $\overline{LE}$ signals are presented (in the lower and in the upper part of the picture, respectively). All these simulations results were done for a LE asymmetric design: both LE and $\overline{LE}$ are connected to an external DC level and to the output of the integrated step through a 2k2 resistor, respectively, but LE is connected to the Q discriminator output through a 47 pF capacitance and $\overline{LE}$ is connected to the $\overline{Q}$ discriminator output through a 27 pF capacitance (different respect to STEP3).

We have also done the simulation for the LE symmetric configuration putting both capacitors at the same value in two different cases: 47 and 27 pF, respectively. In the symmetric case with the 47 pF capacitors the accuracy in the measurements of the digital signal is smaller. The digital signal is wider than in the asymmetric case. However, with real boards the jitter in the measurements of the ToT is higher. The explanation for this effect is that for the symmetric case with 47 pF capacitors the decay of the LE signals is slower and the crossing point between LE and $\overline{LE}$ is flatter than in the asymmetric case. Then, the jitter in the measurement of the width of the digital signal is higher. And for the symmetric case with both capacitors set to 27 pF, the width range of the digital signal is shorter than the others. As consequence, we decided to go to an asymmetric configuration.

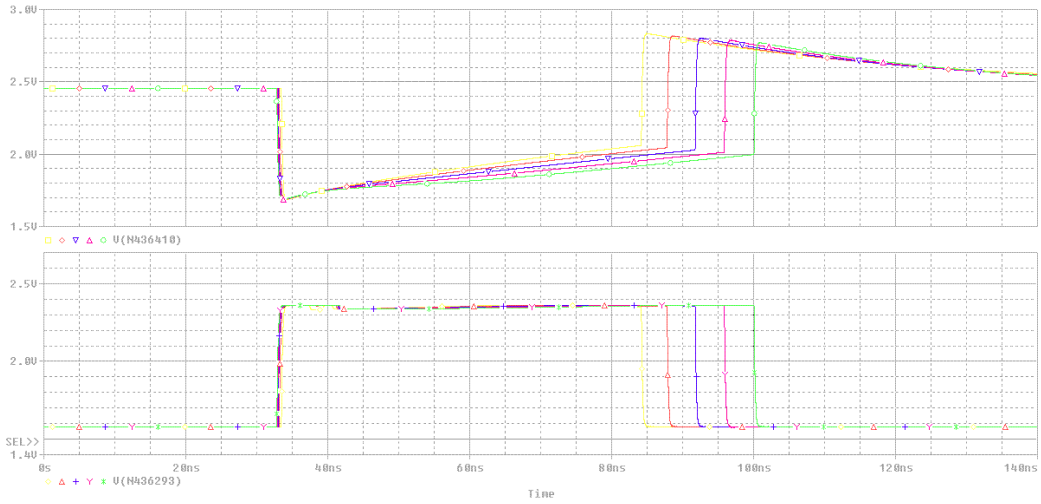


Figure 5.10: *Digital and $\overline{LE}$ signals for different gain values between 50 and 150.*

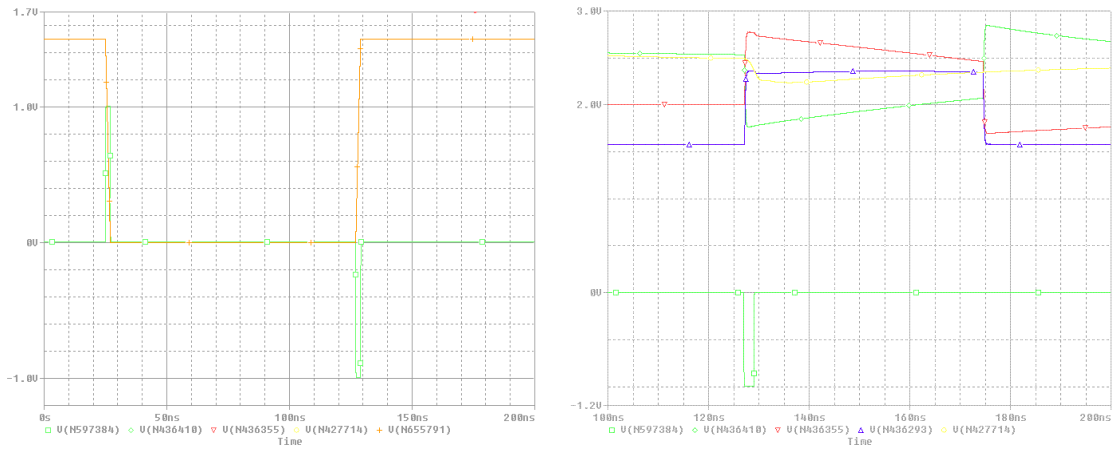


Figure 5.11: *Left: test signal pulse before and after the 1 pF capacitor. Right: response to the negative pulse, showing in the upper part the relevant signals.*

Charge to Width correlation

We have also analyzed the correlation between width of the digital signal and the charge at the input of the preamplifier or the amplitude of the amplified signals. For this purpose two different simulations were done:

1. Injecting test signals at the input of the preamplifier through a 1 pF capacitor.

2. Injecting pulses of different amplitudes directly at the input of the preamplifier.

1. To measure the charge information for the test signals, we injected a known square amplitude input signal with a constant voltage source through the 1 pF capacitor that differentiates the signal producing two peaks: one for the leading edge

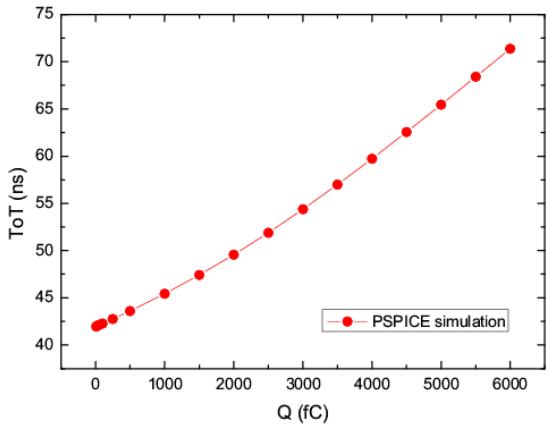


Figure 5.12: *ToT-width as function of the charge for the DBO-STEP5 simulation, showing a rough linear behaviour for normal avalanches.*

and other for the falling edge. We are only interested in the negative one because the discriminator expects negative signals (see Fig. 5.11). The input amplitude was changed for different values between 10 mV and 6 V with this voltage source. The charge value is obtained through Equation 5.5:

$$V = \frac{q}{C} \longrightarrow q = V \times C \tag{5.5}$$

Results corresponding to this behaviour are presented in Fig. 5.12, showing an almost linear behaviour. The charge is measured in fC, taking values between 10 and 6000 fC (corresponding to normal RPC avalanches $\leq$50 mV, also shown at the first region of Fig. 5.5). This correlation shows a possible good behaviour to measure the charge through the width of the interested signal in the real PCB design.

2. In order to estimate the charge of the amplitudes injected at the input of the preamplifier, the amplitude of the amplifier output is measured. For this purpose, the intensity source at the input simulating the RPC signals was changed. The idea of this simulation was to study the correlation between ToT and the input signals for big avalanches and streamers signals. Figure 5.13 shows two pictures: the left side presents the simulation response to big avalanches and streamers together with all the associated signals (analog, integrated, digital and latch enable) and the right side presents a detail of the analog signal with the positive undershoot due to its big charge. This undershoot at the output of the preamplifier produces the same effect in the integrated signal and affects to the ToT-width of the digital output signal.

Figure 5.14-right shows how the time width of the LVDS digital output grows faster for small pulses than for larger signals, due to the saturation of the preamplifier and the integrator for the biggest signals and streamers. This curve is presented as function of the input pulse (μA) because there is a linear correlation between the input pulse and the output of the preamplifier (mV), as it is shown in the left picture

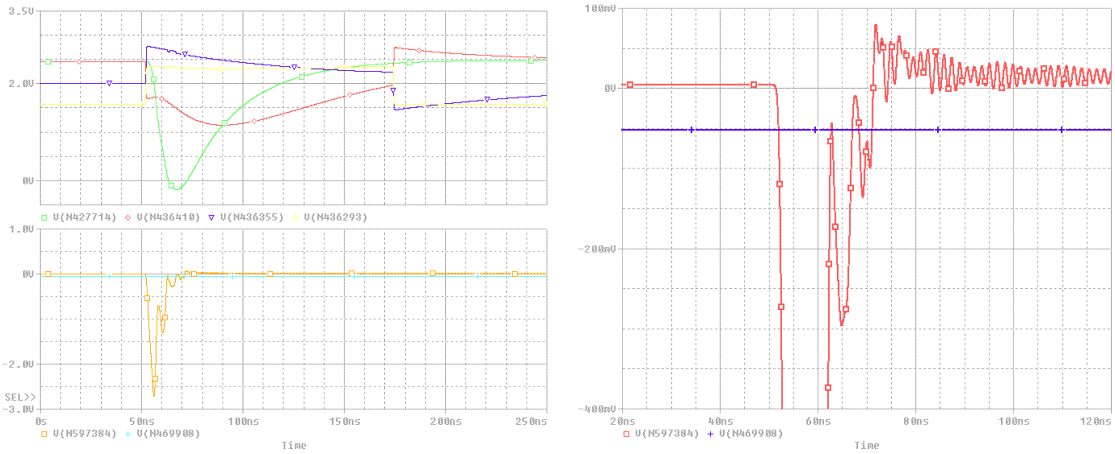


Figure 5.13: *Left: big avalanches behaviour, with all significative signals. Right: analog signal zoom of a streamer, showing its undershoot due to the big charge.*

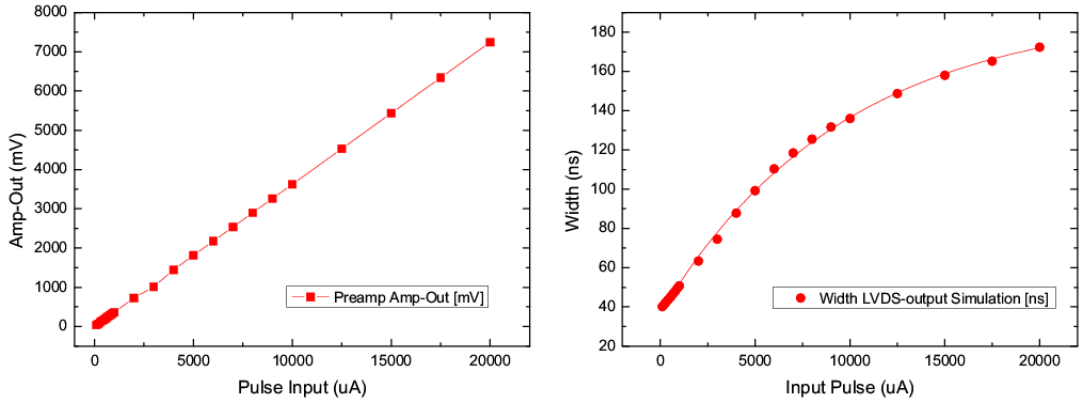


Figure 5.14: *Left: amplitude of the output of the preamplifier as function of the pulse input injected in the circuit, showing a linear behaviour. Right: width of the LVDS output signal as function of the input, showing a saturation for big signals due to the preamplifier.*

of Fig. 5.14. Comparing these results with the ones obtained in Fig. 5.5, in this case the range of the amplitude input is smaller (only until ∼200 mV, taking into account the factor 40 of gain of the amplifier). The minimum ToT value is 40 ns (instead of the 70 ns of the STEP3 simulation). This means that the ToT variation in the linear region is approximately the same in both simulations (70 ns) and the ToT range is bigger for the STEP5 simulation, changing ∼140 ns as comparison with the ∼100 ns of the STEP3. Although the amplifier saturates for amplitudes smaller than the ones at Fig. 5.5, but this could due to the different simulation signals used.

These results were obtained for a default temperature of 27 °C (300 K), but the simulation was also done for different values. The data sheets of the IC guarantee a good behaviour between -40 °C and 85 °C. The simulation also shows a good

behaviour for temperatures between -50 °C and 70 °C, with no significant effects. For values between 70 °C and 85 °C the simulation shows some effects in the baseline of the preamplifier, producing a wrong response in the discriminator output (see results for real temperature tests in chapter 8). However, we do not expect so extreme temperatures, although such high temperatures have some important advantages related with the high rate behaviour of the RPC cells (see chapter 3).

5.3 Simulation conclusions

The simulations explained in this chapter were done facing the optimization of some issues regarding the behaviour of the DBO designs, like the new Latch Enable configuration corresponding to the 'Charge to Width' algorithm (QtoW), but they do not guarantee us the good behaviour of the next FEE designs. Although with the results obtained for the STEP5 we could think in a design close to the FEE needed for the HADES-RPC wall requirements in terms of time resolution, stability, charge information and power consumption [64], [56].

All these aspects about the FEE will be analyzed and discussed in the next three chapters, where the real boards corresponding to both simulations and their different tests (electronic tests or beam times) developed will be presented.

Chapter 6

Development of the FEE-STEP3 and STEP4: design and results

6.1 Introduction to both FEE designs

In this chapter, we present the FEE-STEP3 and its upgrade STEP4 [80] done for the timing RPC wall of HADES. Both designs are very similar, only with small differences. The power consumption was reduced to 0.75 W/channel in both designs, implementing the simulation results obtained for positive pulses presented in the previous chapter.

As it was previously discussed in chapters 3 and 4, the FEE chain requires to cover the wall and to achieve some parameters needed for this HADES upgrade. All the FEE designs are inspired in an earlier board [78] developed in the LIP-Coimbra. The main difference between the FEE-STEP3 and STEP4 and the previous ones (the STEP1 and STEP2 boards) is that in the new STEP3 design the FEE is split in two separated boards in order to fit better with the available room in the keep in volume of the detectors [80]. The layout of this FEE (see Fig. 6.1) consists on two boards [80], [56] and a third one for the acquisition system [86]:

1. A 4-channel DaughterBOard (DBO) [80] implementing two or one fast 1-2 GHz MMIC amplifiers in the STEP3 and STEP4 designs, respectively, feeding a dual discriminator and an amplifier for a charge measurement by a Time over Threshold (ToT) algorithm [49], [50].

2. A 32-channel MotherBOard (MBO) [88], [89] housing up to 8 DBOs, providing voltage supply, DACs for thresholds, test signals, and delivering the differential output signals to a HPTDC [58], [87] placed in the DAQ board.

3. A 128-channel TDC Readout Board (TRB) for the acquisition system [86].

The active DBO [80], developed between the GSI in Germany, the USC in Santiago de Compostela and the CIEMAT in Madrid, and the passive MBO [88], [89], developed between the GSI and the IFIC in Valencia, are presented in next sections.

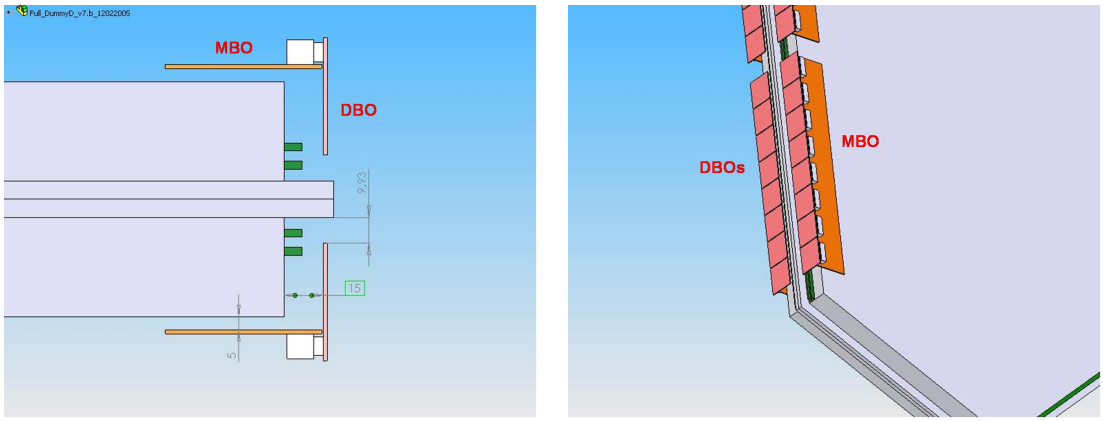


Figure 6.1: *Two different views of the positioning of the FEE setup with respect to the gas box, showing the 8 DBOs in each MBO and a side view of the setup.*

6.2 FEE boards design: DBO and MBO

6.2.1 The active STEP3 and STEP4 boards

The DaughterBOard is a 4-channel and 6-layer board, with an area of 5×4.5 cm^2 (∼22.5 cm^2 in both designs), as shows Fig. 6.2. There are two channels at each side of the board, two on the TOP layer and two on the BOTTOM one. The DBO is the active board which is connected to the RPC cells directly.

As it was explained in chapter 4, in the design of the board (see Appendix B) some special technical issues were needed. In order to control the impedance of the paths as function of their width, thickness and the dielectric constant ε_r (specially in the analog part), the TX-Line programm was used. These both designs were more complicated than in previous boards because these DBOs had six layers, four of them internal, for ground and power planes and also for some paths. When the load is matched to the characteristic impedance of the line some benefits are obtained:

- A transmission line terminated with a load equal to its characteristic impedance transfers an applied pulse to the termination without reflection.
- In this way, all the power of the signal is transferred to the load.

For impedance matching in PCB traces, there are two options [90] (Fig. 6.3):

1. Microstrips. Traces are on the router layers, characterized by an impedance:

$$Z_{DIFF} \approx 2 \times Z_0(1 - 0.48 \exp^{-0.96(\frac{S}{h})})\ \Omega \tag{6.1}$$

where:

$$Z_0 = \frac{60}{\sqrt{0.457\varepsilon_r + 0.67}} \ln(\frac{4h}{0.67(0.8W + t)})\ \Omega \tag{6.2}$$

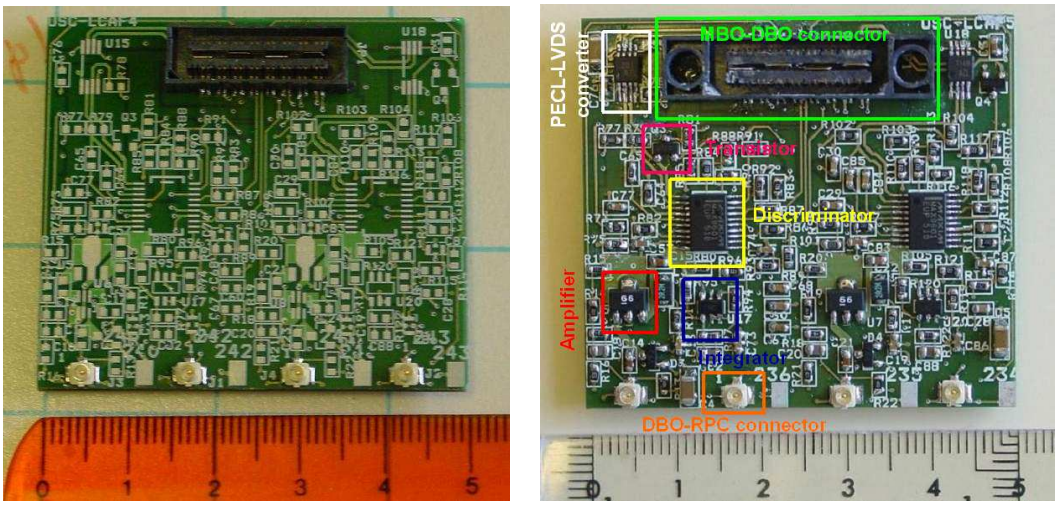


Figure 6.2: *DBO-STEP3 board (left) and DBO-STEP4 board (right), both with four channels (size 4.5×5=22.5 cm^2). The DBO-MBO and DBO-RPC connectors are placed in the upper and the lower part of the board, respectively.*

2. Stripline. Traces are in the inner layers, characterized by an impedance:

$$Z_{DIFF} \approx 2 \times Z_0(1 - 0.374 \exp^{-2.9(\frac{S}{h})}) \ \Omega \tag{6.3}$$

where:

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln(\frac{4b}{0.67\pi(0.8W + t)}) \ \Omega \tag{6.4}$$

In Fig. 6.3, both options are compared: the medium is characterized by a dielectric constant ε_r, S is the distance between traces, h is the thickness of the board, W is the trace width, t is the trace thickness and b the dielectric thickness (between ground planes) in cm. Note that all geometric values must be in the same dimensional units.

For the DBO design, the stripline solution was chosen due to the higher impedance provided by Equations 6.3 and 6.4. This is an advantage also for EMI protection, because ground and/or power planes can be placed on the outer layers. The thickness of the medium cannot be chosen to improve the behaviour because it depends on the manufacturing processes. Distance between traces should be as large as possible to maximize the impedance. An increase of the thickness by factor 2 increases the impedance by 25%. An increase of the distance between traces by a factor 2 increases the impedance by 10%. A reduction of the trace width from W=0.2 mm to 0.1 mm increases the impedance by 1-2%. Other issues were to connect to ground several points of the board using vias to minimize the parasitic inductances and put coupling capacitors to ground as close as possible to the amplifiers.

Main features of the DBO are two amplification stages with a factor of amplification G∼100 for the STEP3 design, and only one with a factor G∼10 for the STEP4,

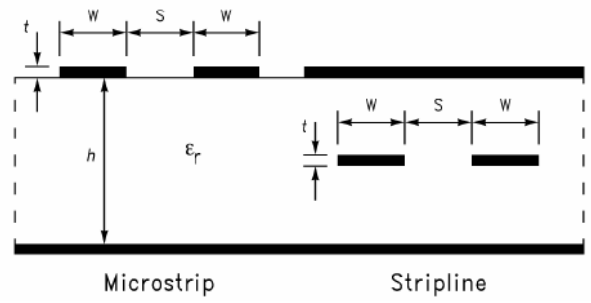


Figure 6.3: *Microstrip and stripline options for impedance matching in a PCB.*

having one LVDS digital output signal per channel to measure the time information and the charge through the Time Over Threshold (ToT) algorithm. The block diagram of the STEP3 is shown in Fig. 6.4, where the part inside the box corresponds to the DBO (the schematics and the layout are shown in Appendix B). This consists of two different sections: an analog and a digital, that we will comment on detail.

Analog section

In the analog stage, since the RPC input signal has frequency components extending up to the GHz range, we have selected Monolithic Microwave Integrated Circuit (MMIC) amplifiers following previous works [28], [47]. This section in the DBO-STEP3 design is based on two different amplifiers in cascade:

- A first preamplifier step based on the Philips BGA2712, a MMIC amplifier featuring 3.2 GHz bandwidth to 3 dB, a flat gain of 21 dB at 2.6 GHz and a good stability (K>1.5) and linearity. This means that the preamplifier has a high gain-bandwidth product (GBW>10^{11}). The frequency analysis of the gain of this amplifier shown in Fig. 4.3 is still valid.
- A second amplifier step based on a Mini-Circuits GALI-S66, a MMIC featuring 2 GHz bandwidth, a flat gain of 18 dB at 1 GHz and a 2.8 dB noise figure. The amplifier has also a high gain-bandwidth product (GBW>10^{11}).

As it was found that the GALI-S66 provided sufficient gain for the RPC signals (a factor $G\sim10$), some of the tests were performed removing the BGA2712. As those tests were successful (results will be shown later), in the DBO-STEP4 board the BGA2712 amplifier was removed. Both amplifiers worked with an impedance of 50 Ω. Then at the input and the output of the amplifier step there is 50 Ω.

The output of the amplifying step was also split in two parallel branches: (a) one goes to an integration stage using a Texas-Instrument OPA690, a wide-band voltage-feedback operational amplifier, and (b) another one goes to the same dual ECL/PECL MAX9601 discriminator, featuring 500 ps propagation delay, where it starts the digital part of the circuit (Fig. 6.4). This integrated signal is used for the charge measurements through the ToT algorithm [49], [50], [80] (see Fig. 4.13).

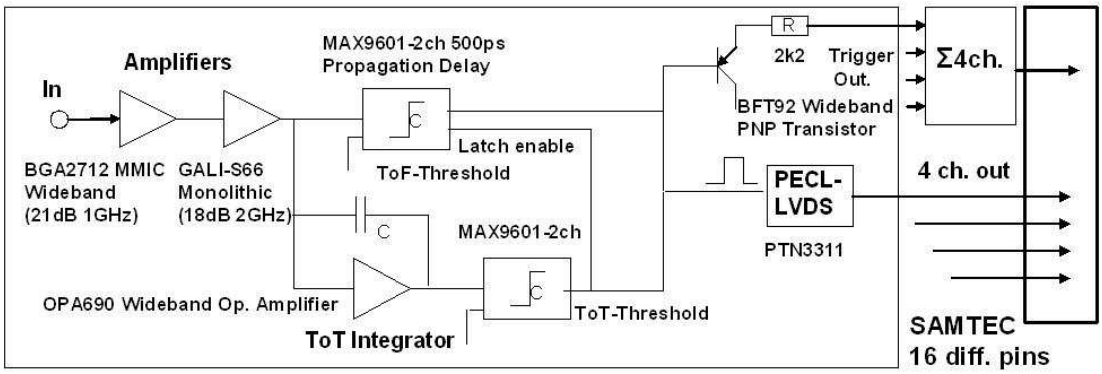


Figure 6.4: *Simplified block diagram of the DBO-STEP3: i) an analog section with two amplifiers connected to an integrator to measure the charge through the ToT and ii) a digital section with an PECL discriminator and a PECL to LVDS converter. The LVDS signal is sent to the DAQ to measure both time and charge.*

Digital section

The design of the STEP3 and the STEP4 digital stages is very similar. The only difference is the converter from PECL signals to LVDS: a Philips PTN3311 in the STEP3 (Fig. 6.4) and a Texas Instrument SN65LVDT100 in the STEP4.

The digital part of both designs starts with a dual ECL/PECL MAX9601 discriminator, the same than in the STEP2. One of this dual comparator is needed for each channel because one discriminator is connected to the output of the analog part for the time information (ToF discriminator with a positive threshold level) and the other one is connected to the output of the integrator signal for the charge information (ToT discriminator with a negative threshold level). And as the second amplifier is inverted, negative RPC signals are needed in the detector.

The leading edge of the digital signal is provided by the ToF discriminator and the latch enable of the MAX9601 discriminator is used to close the PECL digital signal, after a minimum dead time of $\simeq$20 ns for reducing *retriggers* in the discriminator. A PECL to LVDS converter (the Philips PTN3311 and the TI SN65LVDT100 for the STEP3 and STEP4, respectively) follows the discriminator in order to build a digital LVDS output signal the acquisition system needs. These signals are easy to transport even without distortion effects. This was done as is explained in chapter 5 (see section 5.1 and Fig. 5.3), being the width of the digital signal proportional to the charge of the signals through the ToT algorithm [80]. A multiplicity trigger signal for the HADES level-1 trigger is also delivered to the MBO through a summing step of the 4 channels in each DBO. The DBO produces a square signal of 100 mV by each working channel, done with a Philips BFT92 PNP 5 GHz wideband transistor. Later, the MBO makes the analog sum of all the trigger signals coming from the DBOs connected to the board (a maximum of 31 channels and 1.55 V, providing 50 mV by each working channel).

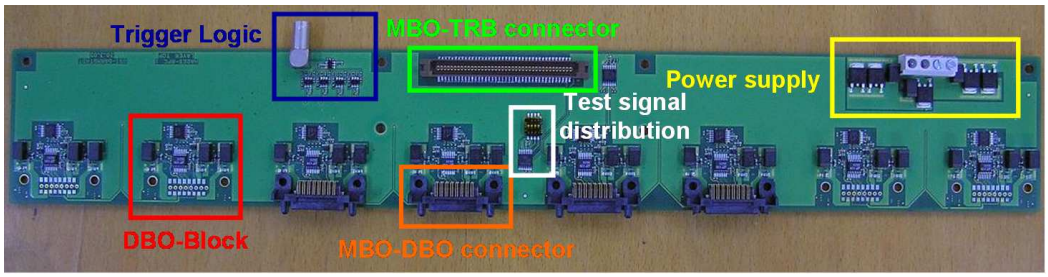


Figure 6.5: *Top view of the MBOv1 with 8×4=32 channels (size 40×6=240 cm^2).*

Connectors

The DBO is connected to the RPC cells through the small connectors placed at the lower part of the board (see Fig. 6.2). These connectors are the U.FL series of the SMT Ultra-Miniature Coaxial Connectors from Wahlström AB, featuring up to 6 GHz (see the reference in www.wahlstrom.se). The connector is soldered to the DBO and covers an area of 7.7 mm^2. The DBO is connected to the detector through a small cable (0.81 mm of diameter) soldered to each RPC cell.

Connectors used for differential line path may also produce impedance mismatch if they are not chosen carefully, producing reflections, increasing crosstalk and worsening the time and charge measurements. For the DBO-MBO connection, we selected the SAMTEC QTS and QSS series. In the DBO side the connector is the SAMTEC QSS with 16 differential pin pairs of 0.635 mm pitch. The connector is specified for a cross-talk $\leq$3.6% and an impedance mismatch of $\leq$10% up to frequencies of 2 GHz (see the reference in www.samtec.com). In the STEP4 board a couple of holes were included in the connector to screw it to the MBO board making the system more stable (Fig. 6.2).

6.2.2 The passive MBOv1 board

The MotherBOard is the board that interfaces the DBOs with the DAQ. The so-called MBOv1 is the first version developed at GSI by S. Lange. It is a 32-channel and 8-layers board housing up to 8 DBOs. The layout is divided in eight separated blocks, one for each DBO to be plugged in. These blocks contain DC filtering for the voltage regulation, an 8-channel programmable DAC[1] and inverters to provide the thresholds that the time-of-flight and time-over-threshold measurements need. The dimensions of the MBOv1 are 40×6=240 cm^2 and a picture of the board is presented in Fig. 6.5, showing the blocks for each DBO. The way in which these blocks are placed on the board is shown in Fig. 6.6.

Other parts of the board are the low level trigger signal output for the HADES acquisition, obtained from the multiplicity signals coming out from each DBO chan-

[1]Digital to Analog Converters.

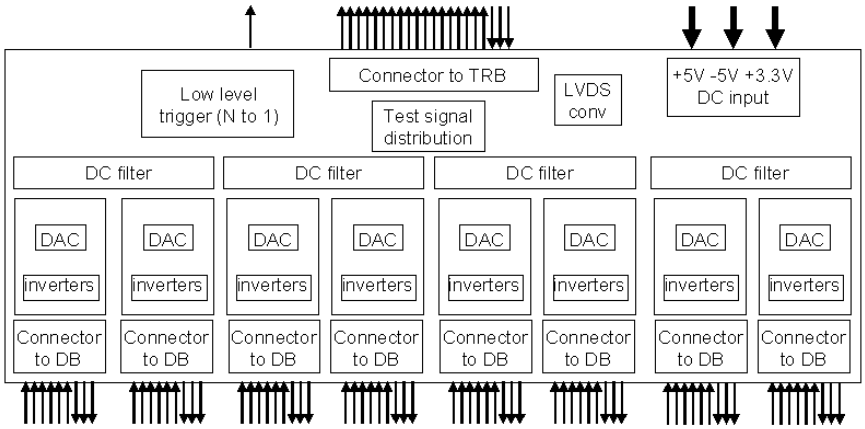


Figure 6.6: *Simplified block diagram of the MBOv1.*

nel, and the LVDS conversion to send the control and test signals to the TRB and the test signal distribution scheme.

Interface for DBO-TRB signal transmission

The MBO provides interface for signals delivered from the DBO to the TRB. Due to the shape of the detector, the TRB cannot be placed next to the MBO. Time-window signals do not have a fix frequency because the pulses appear only when a particle is detected, being the maximum pulse rate estimated to 1 MHz. Since the maximum jitter allowed for the full chain is $\leq$100 ps, the lines must allow the transmission of very short edge signals. The shorter the edge time transmitted the lower the jitter. However, increasing the bandwidth makes the system more sensitive to noise. Then, a robust and immune to noise interface must be used for signal transmission from the MBO to the TRB. This is especially important for the time signals, but also convenient for the rest of control signals (especially for test signals) that are also transmitted though the same cables.

The Low Voltage Differential Signalling (LVDS) Standard [84] is a way to transport data using a very low voltage swing. This differential technology allows single channel data transmission at hundreds of megabits per second (Mbps). Its low swing and current mode driver outputs create low noise and provide very low power consumption across frequency (see Table 6.1). LVDS levels are smaller (50%) than the PECL ones. EMI effects are also reduced, as the signalling swings are much smaller than TTL and PECL due to the current mode drivers, the soft transitions, the low switching currents and the true differential data transmission.

The driver output consists of a current source (3.5 mA nominal) which drives one of the differential pair lines. The receiver has high DC impedance, so most of driver current flows across the 100 Ω termination resistor, generating $\sim$350 mV across the receiver inputs. When the driver switches, it changes the direction of current flow across the resistor, creating a valid *one* or *zero* logic state.

	Industry standard	Maximum Data Rate	Out swing (V_{OD})	Power consumption
LVDS	TIA/EIA-644	3.125 Gbps	±350 mV	Low
LVPECL	N/A	10+ Gbps	±800 mV	Medium to High
CML	N/A	10+ Gbps	±800 mV	Medium
M-LVDS	TIA/EIA-899	250 Gbps	±550 mV	Low
B-LVDS	N/A	800 Gbps	±550 mV	Low

Table 6.1: *Industry standards for various LVDS technologies.*

Differential transmission [91] is practically immune to power supply fluctuations. The differential data transmission method used in LVDS is less susceptible to common-mode noise than single-ended schemes. Differential transmission uses to carry data information two wires with opposite current/voltage swings instead of one wire used in single-ended methods. The advantage of the differential approach is that noise is coupled to both wires as common mode (the noise appears on both lines at the same time) and it is thus rejected by receivers sensitive only to the difference between both signals. Differential signals also radiate less noise than single-ended signals due to the cancelation of magnetic fields.

Impedance matching

The MBO is completely impedance matched to reduce signal reflections and distortions. Connectors were carefully chosen and they are high frequency and impedance matched. In the case of cabling transmission, when the LVDS transmission medium consists on traces on a printed circuit board, the characteristic impedance of the medium must be matched with the termination to complete the current loop and terminate the high-speed lines. If the medium is not properly matched, signals reflect at the end of the cable or trace and interfere with signals coming later. In the case of the MBO, the maximum line distance is about 30 cm. Not matching the MBO represents a risk for signal integrity because it produces impedance mismatching in the time delivery path.

For the MBO design, the stripline solution was chosen because Equations 6.3 and 6.4 provide higher impedance. This is an advantage also for EMI protection, because ground and/or power planes can be placed on the outer layers. As it was explained in section 6.2, the thickness of the medium can not be chosen because it depends on the manufacturing processes. Distance between paths should be as large as possible to maximize the characteristic impedance.

In order to prevent reflections, LVDS requires a terminating resistor of 100±20 Ω that was matched to the actual cable or PCB traces. This resistor completed the current loop and terminates the signal properly. It was placed across the differential signal lines as close as possible to the receiver input. With this termination, an LVDS driver could drive a twisted pair wire over 10 m at speeds exceeding 155.5 Mbps (77.7 MHz). The MBOv1 was equipped with a high-speed differential receiver and

ToF/ToT A low	2	1	ToF/ToT B low
ToF/ToT A high	4	3	ToF/ToT B high
-5 V	6	5	+5 V
-5 V	8	7	+5 V
mult-4	10	9	Test Signal A/B
GND	12	11	GND
Threshold ToF A	14	13	Threshold ToF B
Threshold ToT A	16	15	Threshold ToT B
Threshold ToF C	18	17	Threshold ToF D
Threshold ToT C	20	19	Threshold ToT D
GND	22	21	GND
multiplicity-4	24	23	Test Signal C/D
+5 V	26	25	+3.3 V
+5 V	28	27	+3.3 V
ToF/ToT C low	30	29	ToF/ToT D low
ToF/ToT C high	32	31	ToF/ToT D high

Table 6.2: *Pin-out assignment for the MBOv1 and DBO-STEP3 connector.*

driver, connected as a repeater at the end of the differential lines. This device, the TI SN65LVTS101, accepts low-voltage differential signalling at rates up to 2 Gbps with total jitter lower than 65 ps, including a 110 Ω differential line termination.

Connectors

As was previously discussed in this chapter, a good choice is needed to avoid impedance mismatch. For the DBO-MBO connection, at the MBO side the choice was the SAMTEC QTS series, which are impedance matched connectors with pins distributed in differential pairs signalling. These high-speed connectors provide up to 2 GHz bandwidth in differential mode, which ensures the integrity of the signal transmitted and also provide a right-angle connection for detector geometry reasons. The pin-out distribution is shown in Table 6.2. Signal delivery is carried out on the MBO by cooper traces. Special consideration were taken in the design and routing of these traces to reduce jitter. The time signals were distributed on the sides, separated from the rest of the signals with ground pins shielding and reducing the crosstalk that could be induced by the multiplicity signals. Threshold voltages were grouped together in the middle of the connector because they are low frequency signals, and separated from the multiplicity signals with ground pins.

For the MBO-TRB connector the selection was a KEL8930 series with 80 pins. It is the big connector placed in the center of the MBO (Fig. 6.5). The pin-out collects all differential signals on one side, providing also interface for the SPI[2] communication and test signal (see Fig. 12 in Appendix B).

[2]Serial Peripheral Interface.

Threshold voltages

The discriminators of the DBOs require some thresholds which are important for the accuracy of the time measurement in particle identification. Every DBO channel requires two different thresholds, one for the ToF and other for the ToT. In ideal conditions, the same voltage threshold value would be set for all ToF and ToT discriminators. In practice, thresholds of every single channel must be set separately to correct differences in offsets, gain and noise. This is essential, for example, when a channel becomes noisy and we need to disable it. For this reasons, thresholds must have remote programming capability.

In order to set optimum threshold levels, programmable thresholds were implemented by DACs placed on the MBO. The DAC is the Linear Technology LTC2620 which integrates 8 channels with low power operation, very low crosstalk between channels (<10 μV) and 12-bit resolution. The digital to analog transfer function is given by the following equation:

$$V_{OUT(IDEAL)} = (\frac{k}{2^N}) \cdot V_{REF} \tag{6.5}$$

where k is the decimal equivalent to the binary DAC input code, N is the number of bits and V_{REF} (3 V) is the maximum output voltage.

The LTC2620 used a simple SPI serial interface that allowed to program in a remote way up to 8 DACs through only one input data pin. DACs were connected as shown in Fig. 6.7. Every DAC was set in slave configuration and all of them shared the same clock (CLK) and chip select (CS) signals, controlled by the TRB. The DAC was daisy-chained and the data output of the TRB (SDO) was connected only to the data input (SDI) of the first DAC. In this configuration, the shift register of the devices were connected in serial, forming a single input shift register which extends through the entire chain. The data were transferred to the first DAC, and then shifted to the next device with the rising edge of the clock signal. LVDS to TTL converters were used for transmission of the SPI signals from the TRB to the MBO. In order to reduce noise due to reflections, the LVDS signals were terminated by 100 Ω resistors at the end of the lines for line impedance matching. For SPI programming, the IC select signal enables the slaves (the DAC), and the programming data was sent synchronized with the clock signal in the format:

[Delay(8Bit)+COMMAND(4Bit)+ADDRESS(4Bit)+DATA (12Bit)+DONTCARE(4Bit)]

The ranges needed for the ToF and ToT thresholds went 0 to 50 mV and 0 to 100 mV, respectively. The use of a 3.3 V and a resistor divider by a factor 4 on the DBO allowed for a ToF threshold voltage step of 200 μV in a range of 825 mV. The ToT divider factor was 2.3, being the voltage step 350 μV in a range of 1.4 V.

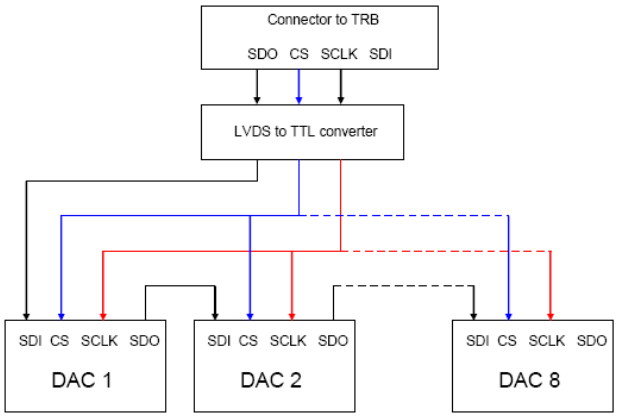


Figure 6.7: *Daisy-chain configuration for the DACs placed on the MBO.*

Power distribution system

The DBO requires three different power voltages: +5 V, -5 V and +3.3 V. All must be extremely stable and with low noise to avoid any interaction with the timing measurement. This is most important on the DBO because it receives low level signals that should be free of noise, taking into account the preamplifier input is the most noise sensitive point due to the small amplitude and width of the signals. The power and ground planes can be a source of noise if they are not treated correctly.

As a power system, the MBO fulfills two essential purposes: to provide stable voltage references for exchanging digital signals and to distribute power to the DBOs. Providing stable voltage levels is based on basic power system design rules [92]:

- Use low-impedance ground connection between gates and a low-impedance path between power and ground.
- The impedance between power pins on any chip should be as low as the impedance between ground pins.

Power supplies sold for use in digital electronics have extremely low output impedances. Across their output terminals, power supplies generally satisfy the first rule. Circuits mounted directly across the power supply output terminals fully benefit from the low impedance of the power supply. Circuits mounted anywhere else must be connected to a power supply by wires or traces. The relatively large inductance of this termed power distribution wiring raises the low output impedance of most power supplies. Measured at the end of the power distribution cable, DC regulation may still be very good, but high frequency impedance is often too large.

In order to avoid the problems created by power distribution wiring inductance, large bypass capacitors should be placed on each printed circuit card. This capacitor was connected in parallel to the power supply. In the frequency range where wiring inductance starts becoming a problem, the bypass capacitor provide a low impedance

	Input (V)	Output (V)
No signal detected	3.1	0
Signal detected	2.4	-3.2 (all channels fired)

Table 6.3: *Voltage levels at the input of the trigger stage (output of the DBOs).*

between power and ground. At some even higher frequencies, the bypass capacitor losses its effectiveness as a consequence of the inductance of its mounting leads.

In order to fix inadequacies of a large bypass capacitor, an array of other smaller bypass capacitors was included. The capacitor array picked up where the big bypass capacitor left off. Although the array had a capacitance smaller than the big bypass capacitor it had a lower series inductance. The combination of the power distribution wiring, the big bypass capacitor and the small bypass capacitor array (called a multilayered power distribution system) working together provides a low impedance power source for every logic device across the whole operating frequency range.

Test signals

For calibration and testing, each MBO provides interface for the transmission of an internal pulser system common to all 32 DBO channels which can be en/disabled by software. Test signals generated on the TRB are delivered by a LVDS driver through a ribbon cable to a connector placed at the center of the MBO (Fig. 6.5). As was previously explained, test signals were transmitted as LVDS signals and were converted into CMOS[3] to get the logic levels needed to test the channels. A differential de-multiplexer on the MBO, the MAX9169, distributed the test input signals, which could be sent to all channels or to odd and even channels separately. Channels for signal delivery could be selected through a DIP-switch. Before going to the DBO test input these signals were converted into narrow pulses through a passive RC derivative circuit placed behind a MAX9130 TTL receiver.

Additionally, a probe temperature sensor was implemented on the MBO side for monitoring the temperature during the experiment.

Low level trigger output

The data acquisition system requires a trigger signal which provides information about the number of channels fired in the whole detector for each event. In the MBO, trigger information of every DBO channel is collected in a single trigger signal used for low-level triggering, which is sent to an output. This trigger signal is implemented by a summing stage with the interface voltage levels given in Table 6.3. The maximum output level fits the maximum voltage required by the TRB input.

A DBO channel provides 2.4 V and 3.1 V to the trigger when signal is fired or

[3]Complementary Metal Oxide Semiconductor.

First stage	Input (V)	Output (V)
No signal detected	3.1	0
Signal detected	2.4	1 (all channels fired)
Second stage	Input (V)	Output (V)
No signal detected	0	1
Signal detected	0	-1.5 (all channels fired)

Table 6.4: *Levels for both trigger summing stages.*

not, respectively. The input voltage levels correspond to the LVPECL[4] levels from the output of the DBO discriminators plus the 0.7 V collector-emitter voltage drop in the transistor (which buffers the trigger signal to the summing stage).

The summing stage is composed of two parts: four summing amplifiers and a summing amplifier working in cascade, placed at the MBO in the lemo connector area (Fig. 6.5). The operational amplifier OPA690 was selected for the low level trigger mainly because of its high slew rate (1800 V/μs) and its high output swing ($\pm$4 V). Each DBO channel must produce a contribution of -100 mV at the output of the trigger. As the number of channels contributing to generate this trigger signal is 32, the output voltage with all channels fired is -3.2 V, which is the output required by the TRB when all channels fire simultaneously.

Although in order to obtain the widest bandwidth from the OPA690 amplifier its gain should be set to 1, we decided to set it to 1.5 to provide a safer phase margin and to improve stability. This value was set with different resistors. For a gain of 1.5, the input and output levels of the first summing stage are shown in Table 6.4.

The second stage sums the result of the four previous operational amplifiers. Choosing the same gain value of 1.5, the input and output voltages in this stage are shown in the last column of Table 6.4. As consequence, every signal detected in a channel contributes to the trigger signal at the end of the second stage by -50 mV.

6.3 The acquisition board: the TRBv1

The DAQ system of the new HADES RPC wall is based on the TDC Readout Board (TRB) [86], developed at GSI as a general purpose trigger and readout board with on-board DAQ functionality. A picture of this board is shown in the left side of Fig. 6.8, together with a block diagram of the board.

The TRB implements four 32-channel High Performance Time-to-Digital Converter (HPTDC) [58], [87], designed by the electronics group at the CERN with a time resolution of σ_T=40 ps/channel. The main usage of the first version of the board, the so-called TRBv1, was to read out the RPC detector of the HADES upgrade ($\sim$2500 FEE channels) [86], with a time resolution σ_T<100 ps and the pos-

[4]Low Voltage Positive Emitter-Coupled Logic or Low Voltage PECL.

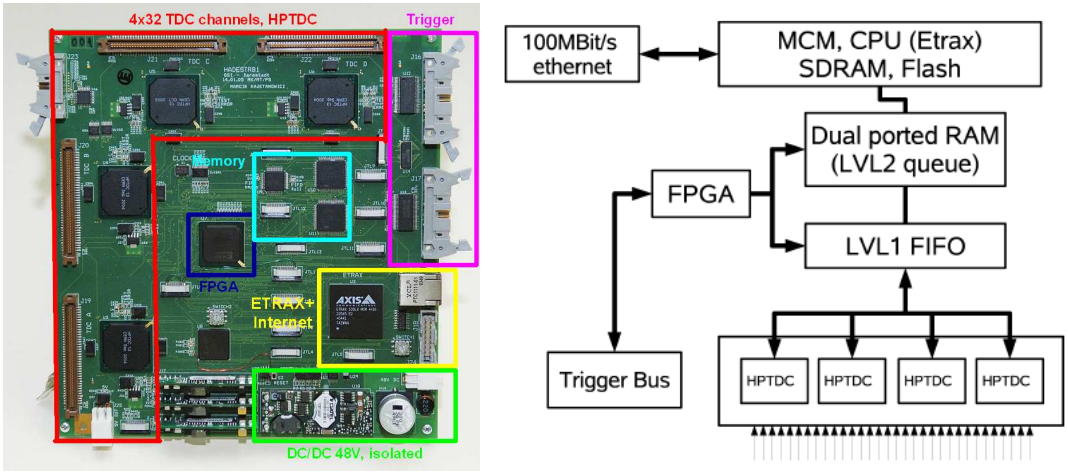


Figure 6.8: *Left: top view of the TRBv1, 4×32 channels (its size is 20×23 cm^2). Right: block diagram of the TRBv1, showing its main features.*

sibility to measure both the time of the rising and falling edge of the signal to make a Time Over Threshold (ToT) measurement for a walk-correction of the cell.

The Time to Digital Conversion of the 128 channels is done in four HPTDC chips (see Fig. 6.8-right). The TRB has four input connectors (80-pins with high density), each of them with 31 LVDS timing input signals and several I/O-signals for general purpose. The 32nd channel of each HPTDC is connected to an external reference timing signal (LVDS). The HPTDC ASICs are highly configurable [87] and allow to choose the TDC bin-width in the range of 780 ps and 25 ps (at 25 ps only a quarter of the channels is available), to detect the rising and falling edges of the timing-signal allowing to define a matching-window. The multi-hit capabilities offer the possibility to measure the Time-over-Threshold (ToT) and thus to obtain pulse height information of the detector signal.

An external trigger signal starts the selection of data in the HPTDCs and the board-controller FPGA initiates the readout. These data are first stored in the LVL1-FIFO (with a capacity of 128 kB) where they wait for an external LVL2 trigger decision, which decides if the data can be discarded or has to be transported to mass storage (the LVL2 trigger is needed for the HADES DAQ but optional). If the trigger was positive, the data are stored in a second dual-ported memory (128 kB) or discarded. The data are then read out by a single IC processor (ETRAX[5] [93]) running linux. The data are formatted and transported via UDP internet protocol over 100 MBit Ethernet to the event-builder, which collects and orders the individual sub-events from all readout chains of the spectrometer. The UDP internet protocol transport performance of the ETRAX has been measured to be 11 MB/s. With a pulser, we achieved rates of 80 kHz on LVL1 (with large down scaling) and up to 18 kHz LVL2 rates, which corresponds to data rates of 1.8 MB/s.

[5]Ethernet, Token Ring, AXis.

Having the DAQ-system with a full featured computer so close to the FEE allows the implementation of the slow-control for setting all the threshold levels of the FEE on the TRB with EPICS[6] [94], a set of Open Source software tools, libraries and applications developed and used worldwide to create distributed soft real-time control systems for scientific instruments. The TRB uses a 48 V galvanic isolated power-supply which simplifies power-distribution, prevents ground-loops and allows to mount the TRB directly on the detector. The time resolution calculated from the time difference between two reference channels (different HPTDCs) was σ_T=40 ps (with 100 ps binning), as expected from the HPTDC performance [87]. Great care was taken in the design of the PCB layout to assure impedance matched and decoupled transmission lines of the LVDS-timing signals, which limited additional crosstalk effects to the overall time resolution of 40 ps to less than 20 ps.

6.4 FEE-STEP3 performances analysis

The performances of the FEE-STEP3 and the STEP4 and the whole chain were analyzed both with test signals and RPC signals, looking at the following features:

- The time resolution of both systems.
- The crosstalk between channels (measured as the influence of one fixed channel in another one that is not connected to the RPC [79], [80]).
- The charge of the RPC signal measured through the ToT algorithm.

The experimental setup implemented for all these tests is similar to the one used with previous boards (see section 4.3.1, Fig. 4.4), using a Digital TEKTRONIX TDS7104 series oscilloscope with 1 GHz bandwidth. Measurements were developed both at LabCAF laboratory in the USC and at LIP laboratory in Coimbra.

6.4.1 Time Resolution

Regarding the time resolution tests, two kind of measurements were done using:

1. Narrow signals coming from a 600 MHz bandwidth pulse generator injected through the test input of the FEE.
2. Real RPC signals from the same prototype used in previous tests [64], [65].

Figure 6.9-left shows the two basic components which deteriorate a time measurement [95]:

1. The slewing correction or 'Walk', which is due to the amplitude variation of the input signal for a nearly constant rise time of the primary signal.

[6] Experimental Physics and Industrial Control System.

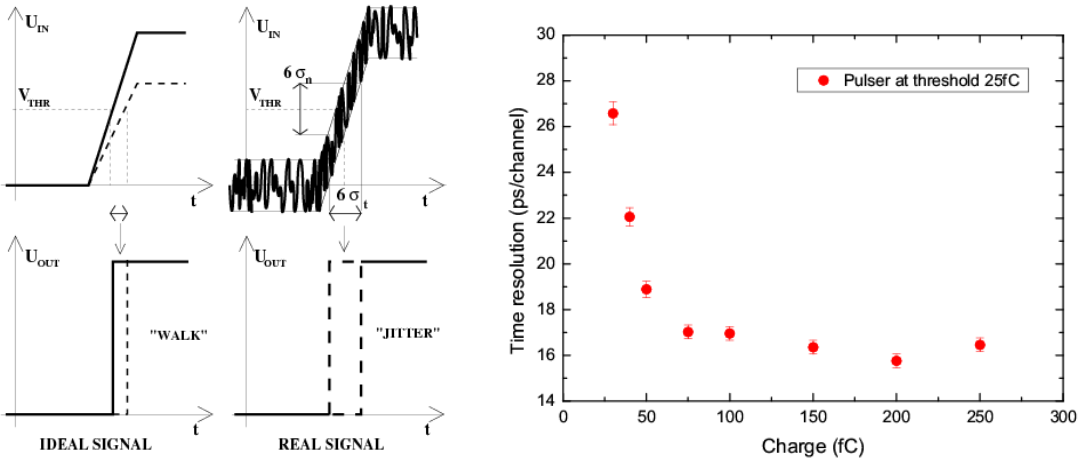


Figure 6.9: *Left: two main components which deteriorate a ToF measurement. Right: FEE-STEP3 time resolution per channel measured with fast pulses.*

2. A more important point is the so called 'jitter', dominated by the noise of the amplifier. The noise dispersion σ_n at the leading edge projected onto the time base allows to estimate the electronic resolution. In general, there exists a second additive term, the intrinsic jitter δ_t, which is due to the discriminator and the time digitizer, so the whole jitter can be expressed by [53]:

$$\sigma_{te} = \frac{\sigma_n}{\frac{dV}{dt}} + \delta_t \tag{6.6}$$

In order to reduce this component, the noise-to-slope ratio has to be minimized. If we assume a uniform distribution of the noise (white noise) with a spectral density $N_d\,[V^2/Hz]$ for the frequency band BW $[Hz]$ we get $\sigma_n^2{=}BW \times N_d$, if the preamplifier has a single pole $t_r{=}\frac{0.35}{BW}$. With a signal amplitude A one obtains $\frac{dV}{dt}{=}0.8 \times \frac{A}{t_r}$ and the minimum electronic resolution due to the jitter can be estimated by:

$$\sigma_{t(FEE)} \sim 0.44 \times \frac{\sqrt{N_d}}{A \cdot \sqrt{BW}} + \delta_t \tag{6.7}$$

In order to decrease this jitter provided by Eq. 6.7 even further, the amplifier requires a low noise and a high bandwidth. Additionally, the pick-up of parasitic signals has to be minimized by the proper design of the PCB and of the interface between the detector and the electronics. For this purpose we use the flexible RF coaxial cable with a small impedance variation (50±1 Ω) and an impedance-matched RF connector (50 Ω) to connect FEE and detector.

Time resolution of the FEE with test signals

For the measurements of the FEE time resolution as function of the charge, the charge at the input of the electronic channel was calculated with Eq. 3.1. The DBO

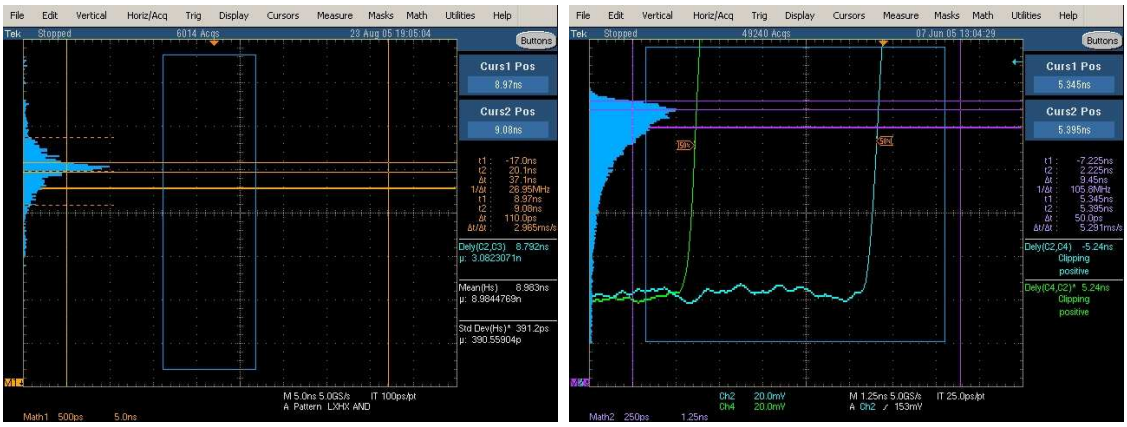


Figure 6.10: *Time resolution measured for the RPC and the FEE. Left: for a point-like illumination. Right: illuminating one edge of the detector.*

had four channels, each of them with its own test input with a voltage divider of a factor 10 and a capacitor of 1 pF. An external square input signal with 1 μs width and amplitude varying between 500 mV and 2.5 V (maximum value) generates on the DBO channel two narrow signals of a few ns width. In order to inject these signals through the test input, a miniMBO was developed by our group, a reduced version of the MBOv1 for testing DBOs individually with a similar design. It provided to the DBO all the voltage supplies, the threshold levels and the input for external pulse signals (see Figures 13 and 14 in Appendix B).

Results of the time resolution of the STEP3 as function of the charge with test signals are shown in Fig. 6.9-right. The so-called jitter is dominated by the noise of the amplifier. As we do not know the specifications of the pulse generator, we can only determine the combined intrinsic resolution for the whole setup. The average time resolution for charges higher than 50 fC is $\sigma_{T(FEE)}$~16 ps/channel, making worst for lower signals (~30 ps/channel for Q~25 fC). The ToF threshold was set at ~25 fC and the ToT at -35 mV. The error in these σ measurements was ~2%.

Time resolution of the whole chain RPC and FEE

In the tests developed with the whole chain, the FEE was placed directly over the RPC for improving the grounding, connecting two channels of the board to both end of the same RPC with a lemo connector, soldered in one side of the SMT miniature coaxial connectors. The cell was illuminated with a ^{60}Co source and the HV applied to the cells was 6000 V. For these tests, two kind of measurements were done:

1. Through a point-like illumination with a γ source in coincidence with a scintillator. The width of the time difference distribution is the electronic jitter.

2. Through the analysis of the signal shape at the RPC edge illuminated with a γ source, estimating the jitter through the smoother of the edge of the cell.

1. The standard way to measure the time resolution is measuring the time difference between the signals at both ends of the same cell when the RPC is exposed to a point-like source. Then, the common effects in the formation of the avalanche cancel reciprocally and only the jitter of both times contribute to spread out the difference. For this purpose the source should be focalized correctly, but it is very difficult to guarantee a real 'point-like' irradiation over the cell with a ^{60}Co source. A measurement done with this method is shown in the left side of Fig. 5.10. The full width at half maximum (FWHM) measured was Δt=110 ps and as:

$$\sigma = \frac{FWHM}{2.35} \tag{6.8}$$

we get a σ_T=47 ps combined for two channels. This means a time resolution of $\sim$33 ps/channel for the whole chain FEE and RPC.

2. A method to overcome this effect is illuminating the cell with the source at one of the edges. If there were no electronic jitter, the time difference distribution should show a sharp-end cut at both ends of the RPC. But if there is jitter, the cut becomes smoother taking the shape a gaussian tail and the time resolution of the whole system can be measured. As is shown in Fig. 6.10-right, we got at the FWHM a $\frac{\Delta t}{2}$=50 ps. Applying Eq. 6.8, we get a σ_T=43 ps combined for two channels, $\simeq$30 ps per channel. The time resolution measured for all the boards varying between 30<σ_T<50 ps/channel. Similar results were obtained for the STEP4.

6.4.2 Crosstalk between channels

In order to study the crosstalk between channels of the same DBO, we measured the time resolution of all the possible pair combinations and different arrival times. The average value was determined as σ_T=40 ps/channel for the whole chain, changing between 30 ps and 50 ps, depending on the proximity of the channels in the board (channels in the same layer or not).

Furthermore, we measured the ratio of signals in a channel not connected to the RPC induced by its neighbour channel connected to the RPC. The crosstalk level was confirmed to be below 1%. The degradation of the time jitter for gamma photons can be explained by the steep charge distribution [96], resulting from an increased population of avalanches close to the threshold. Moreover, no effects were observed in the time jitter due to possible fluctuations of the base line at the output of the analog part that could affect the discriminator's behaviour.

6.4.3 Charge and Time Over Threshold correlation

Two kind of measurements were done for analyzing the ToT behaviour, using:

1. Narrow signals coming from a pulse generator injected through the test input.

2. Real RPC signals from the same prototype used in previous tests [64], [65].

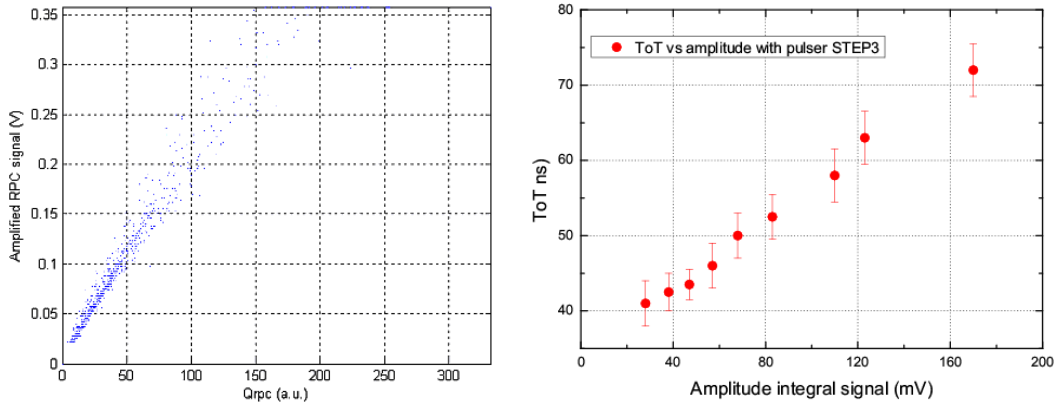


Figure 6.11: *Left: behaviour of the amplitude of the RPC signals vs the charge. Right: correlation between ToT and amplitude of the integrated signals with pulser.*

The ToT [49], [50] is an algorithm to codify the charge of the signals in the LVDS output signal. First, the input pulse is integrated to get its charge and then the LVDS signal is built making its width proportional to the value obtained. This width (Δt) is the width of the integrated signal at a threshold level (see Fig. 4.15-left). The integration stage shown in Fig. 4.12 was still valid, although the differential shaping at the input was removed because different tests show that was unnecessary.

1. For the tests done with a pulse generator, the ToF threshold was set to different values, starting at 10 mV. The ToT threshold was also changed between -10 and -50 mV, being -10 mV the minimum value because the integrated signal was very small and the signal was indistinguishable with the noise level. Test signals of different amplitudes were used, corresponding to different charges at the input of the channels. For each charge the width of the LVDS output signal was measured.

Figure 6.11-left shows the relation between the amplitude of the amplified signals from an RPC and the charge measured with the reference FEE [78] and an external ADC. The high correlation means that we could measured the charge measuring the amplitude. Fig. 6.11-right shows the relation between the amplitude of the integrated signals and the ToT, measured with test signals. The ToF threshold was set to 10 mV and the ToT one to -30 mV. It shows a good linearity between the ToT-width and the amplitude of the integrated signal. The integration constant of the amplifier was set to RC_{int}=2 ns, and the discharge constant to RC_{dis}=20 ns.

2. Regarding the tests done with real signals, a board was used illuminating the RPC with a point-like ^{22}Na source and analyzing the correlation between the ToT-width and the charge. For this purpose, three different signal are needed: two of them from the STEP3 (the integrated and the LVDS signals) and one from the reference FEE (the output of the ADC buffer). In order to define the range of thresholds needed for these tests, we applied the condition to have, simultaneously, a signal in both the ToF and the ToT discriminators. The 'minimum avalanche

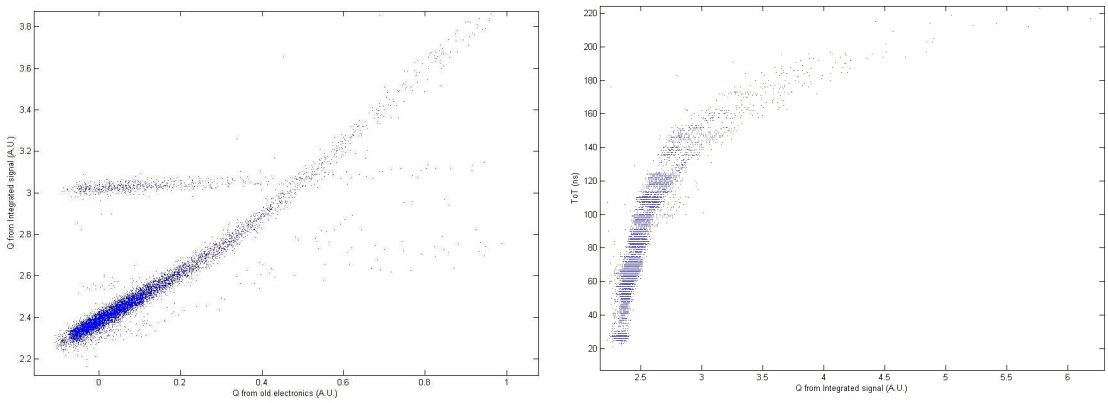


Figure 6.12: *STEP3 board. Left: relation between RPC charge measured on the integrated signal and the charge measured with the reference FEE. Right: ToT behaviour as function of the charge measured on the integrated signal.*

of interest' chosen depended on the design, because STEP3 has two amplifiers and STEP4 has only one. This condition can express through the efficiencies as:

$$\varepsilon_{ToF} = \varepsilon_{ToT} \tag{6.9}$$

Fig. 6.12-left shows the correlation between the charge measured through the integrated signal of the DBO and the charge obtained with the ADC. The dependence is linear for normal avalanches reaching a saturation effect for bigger avalanches. Some low amplitude signals show an odd behaviour giving big amplitudes.

As the correlation is quite clear, we measured also the correlation between the ToT-width and the charge measured through the integrated signal (Fig. 6.12-right). This correlation presents a first order exponential behaviour, showing a higher dispersion for streamers and big avalanches and also a saturation effect at this region. The saturation effect is due to the amplitude saturation of the amplifiers for streamers signals. The ToF and the ToT thresholds were set to 8 mV and -35 mV, respectively. In ToT measurements, the width of the LVDS signals was always bigger than the width of the integrated signal at the ToT threshold level, due to the minimum ToT-width of 20 ns. This pedestal is shown in Fig. 6.12-right and it has to be subtracted to get the charge information of the signals.

6.5 HADES RPC Nov05 beam test at GSI

In November 2005, a prototype of the RPC wall with 24 cells was tested at GSI under secondaries coming from collisions of a Carbon beam impinging on a Lead target. Together with the detector, the mechanics, the FEE and the TRB were also tested for the first time in beam. Very encouraging results were achieved in time resolution and in TRB-Data Acquisition behaviour, being presented in this section.

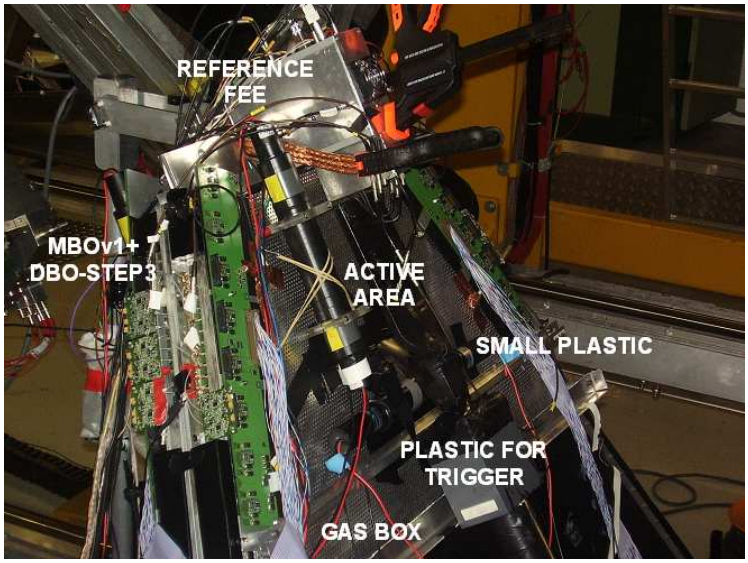


Figure 6.13: *Experimental setup of the 24 RPC cells box used in the beam test.*

6.5.1 Experimental setup

As was mentioned above, a prototype setup of 24 RPC cells following the design explained in chapter 3 was mounted into the HADES frame and tested with particles coming from reactions of 1.5 AGeV ^{12}C beam, with different intensities, on a Pb target. The DBO-STEP4 and the MBOv1 boards were used, together with some STEP3 boards to compare the results. For the acquisition we used the TRBv1. The cells were staggered in two layers covering the low angle region where the highest rates were expected: 13 cells in the front layer (upstream) and 11 cells in the back layer (downstream), as Fig. 3.10 shows.

In a first period, three cells were instrumented, two in the front layer and one in the back one, corresponding to 6 electronic channels, three channels in each DBO. Each DBO was connected to one MBOv1 and therefore to a different TDC in one TRB. In a second period, eight cells more were connected (the central ones), corresponding to 16 FEE channels. Thresholds for the discriminators were changed from run to run and the different behaviours were analyzed. Around two million and eight million of events were taken in the first and the second periods, respectively.

The trigger signal was given by a fast scintillator placed in front of the gas box (upstream), covering the active area of some RPC cells (Fig. 6.13). Complementary data were taken in some other cells instrumented with the reference electronics developed by the LIP [78], [38] and a local trigger was implemented with two scintillators connected to a VME crate. The results achieved with this electronics have been extensively commented in [97], [98], [83], [99]. We used the standard gas mixture [38] and the working point in the High Voltage applied to the central electrodes was set to 6200 V, which means 110 kV/cm (2 gaps of 0.280 mm each).

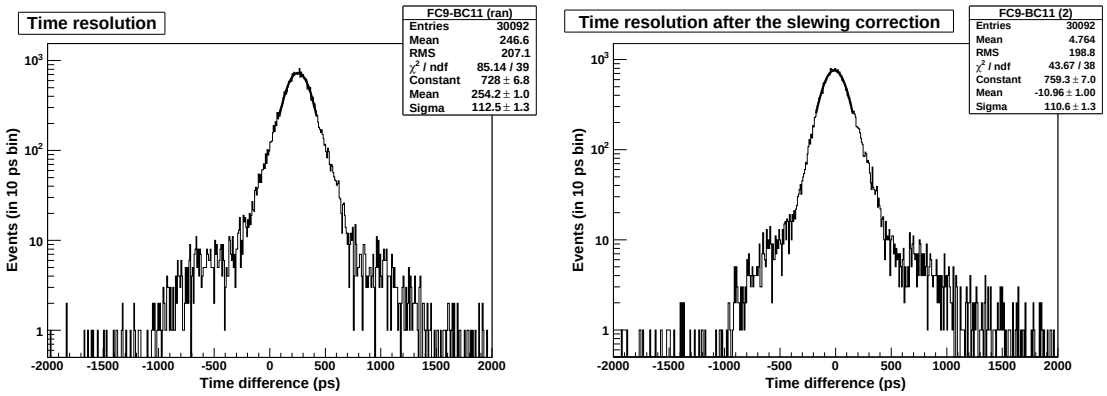


Figure 6.14: *Time resolution measured for the whole chain in beam before (left) and after (right) slewing correction.*

As it was also the first time that the TRB was installed in the HADES spectrometer, a new software was tested. This code was written and implemented in the HADES analysis framework, called HYDRA (Hades sYstem for Data Reduction and Analysis) [100], allowing the use of the full HADES event reconstruction chain. Once data were reconstructed and stored, analysis macros based on ROOT [101] and MATLAB frameworks were developed.

6.5.2 Time resolution measurements

One of the most important aims in this test was to analyze the time resolution measurement of the whole RPC-FEE-TRB chain. The overlap configuration between cells in both layers made it possible. Due to the small distance between layers, the fluctuations in the time-of-flight of particles between them is negligible as compared to the time jitter of the full electronic chain. Then, the width of the tof differences measured at both layers is a good estimation of the composed time resolutions. In order to compensate the effect of the arriving position of the particle in the cell, the estimation is done with the sum of the times measured at both ends of the cell (Fig. 6.17, left). The time-of-flight between layers is given by Eq. 6.10:

$$\Delta t = tof = \frac{t^1_{left} + t^1_{right}}{2} - \frac{t^2_{left} + t^2_{right}}{2} \tag{6.10}$$

where t^1 and t^2 are the times measured at two overlapped cells in the front and back layers, respectively. The time resolution is given by the sigma of such Δt distribution. In a first approach, the accuracy of this difference analysis is dominated by the TDC bin, which was 100 ps. This means a variance of $\frac{100}{\sqrt{12}}$ ps in each TDC.

It is well known that in RPCs there is a systematic shift of the measured ToF at fixed velocity of the primary particle which depends on the avalanche size or charge [22], [37]. This effect can be subtracted through the 'slewing correction'. The charge measurement provided by the ToT-width allows to make such correction.

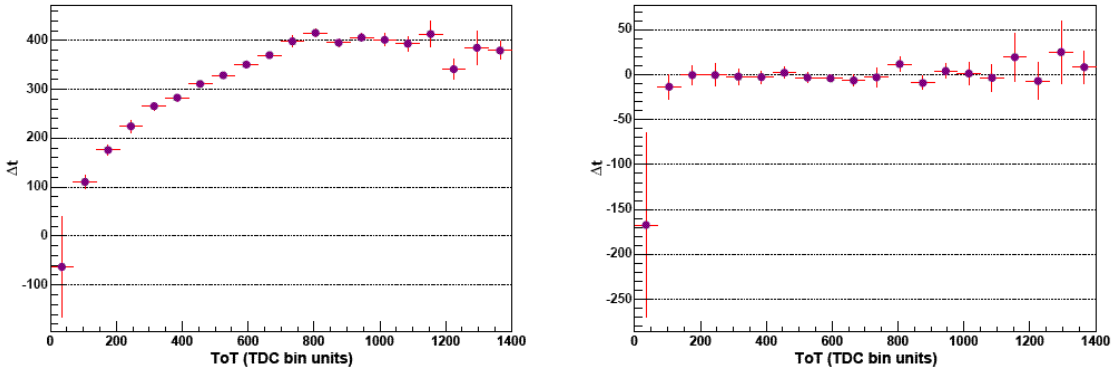


Figure 6.15: Δt *from Equation 6.7 as a function of the ToT value before (left) and after (right) applying the slewing correction.*

Figure 6.14 shows the time difference distribution using Eq. 6.10 before and after the slewing correction. The left side shows an uncorrected combined resolution for two RPC cells of σ_T=112 ps, providing a single cell resolution of $\frac{112}{\sqrt{2}}$=80 ps. In the right picture, the single RPC resolution was reduced to σ_T=77 ps after corrections.

Figure. 6.15 shows the time difference Δt as a function of the ToT before and after applying the slewing correction, respectively. We get improvements in the slewing correction smaller than the ones achieved with the same prototype using the reference electronics. These measurements where developed at LIP in Coimbra [102] and resolutions of 75 ps uncorrected and 55 ps after the slewing correction were obtained. The difference can be attributed to two different factors:

1. A different acquisition mode was used in [102] with a 50 ps TDC bin and separate ADC charge measurements.

2. The resolution of the ToT measurement was not optimized yet. This is one of the aims we have to improve in the final design.

An important feature is that the slewing correction applied to the data removes the contributions of the 3-σ tails from 4.5% to 3% after correction. This improvement can be important in the future for the identification of slow particles like kaons.

6.5.3 ToT-charge measurements

As was previously explained, the resolution of our ToT algorithm was not optimized and should be improved in the final design to provide a better time resolution after the slewing correction.

Fig. 6.16-left shows a typical ToT spectrum (in TDC bin units); it shows a small structure at low ToT values. The right picture shows that the ToT measured at both sides of the same cell are highly correlated. The small structure observed at low ToT values is correlated at both sides. At high ToT values, the measurements show some differences that should be corrected.

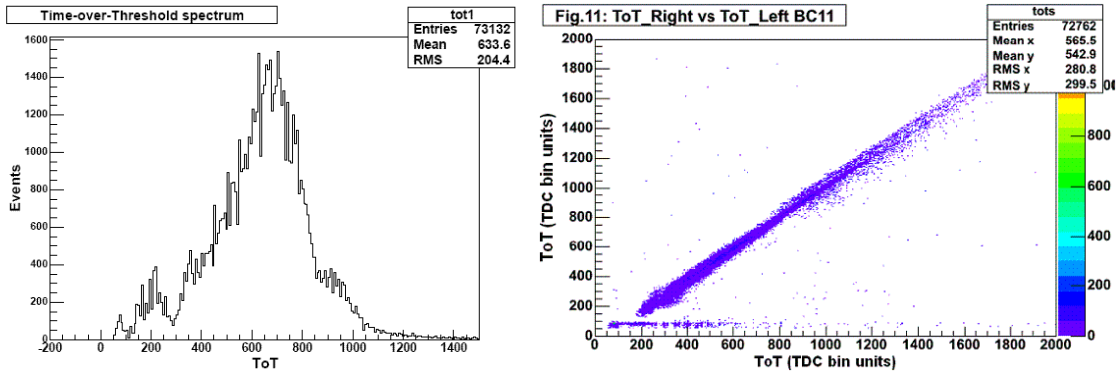


Figure 6.16: *ToT spectrum at one cell side (left) and ToT right versus ToT left (right) of both ends of one RPC cell.*

6.5.4 Position resolution measurements

Although the main goal of the HADES tRPC wall is to offer good timing performances for trigger and time-of-flight purposes, it can provide also the position of the incident particles, helping to the tracking procedure. For this purpose, a good position resolution is needed. The position can be calculated through the time difference between both RPC ends with the expression:

$$x = \frac{t_{left} - t_{right}}{2} \times v_{prop} \tag{6.11}$$

were v_{prop} is the velocity of propagation of the signal inside a tRPC cell. It was analyzed and measured yielding a value of $v_{prop} \simeq 2/3$c [22].

Using two overlapped cells, it is possible to make an estimation of the position resolution achieved with the HADES tRPC [22], [99], which can be derived from:

$$\sigma_{pos} \sim \frac{v_{prop}}{2}\sigma_t \tag{6.12}$$

where σ_t is the width of the electronic jitter associated to the difference of two overlapped cells:

$$\Delta t_{det1} - \Delta t_{det2} = (t^1_{left} - t^1_{right}) - (t^2_{left} - t^2_{right}) \tag{6.13}$$

The histogram of Equation 6.13 for two overlapping cells is plotted in Fig. 6.17. A combined σ_t=170 ps corresponding to a single RPC resolution of $\frac{170ps}{\sqrt{2}}$=120 ps was measured for the central peak. Translated into position by Eq. 6.12, the position resolution integrated over all positions along the cell is $\sigma_{pos}\simeq$12 mm.

Previous measurements done with a similar prototype [22] gave a resolution of σ_{pos}=6 mm, indicating that now we are dominated by the electronic jitter. The width of this cell is ∼20 cm, corresponding to the width of the main peak (≃2 ns). Fig. 6.17 also shows a big background, whose width corresponds to two times the

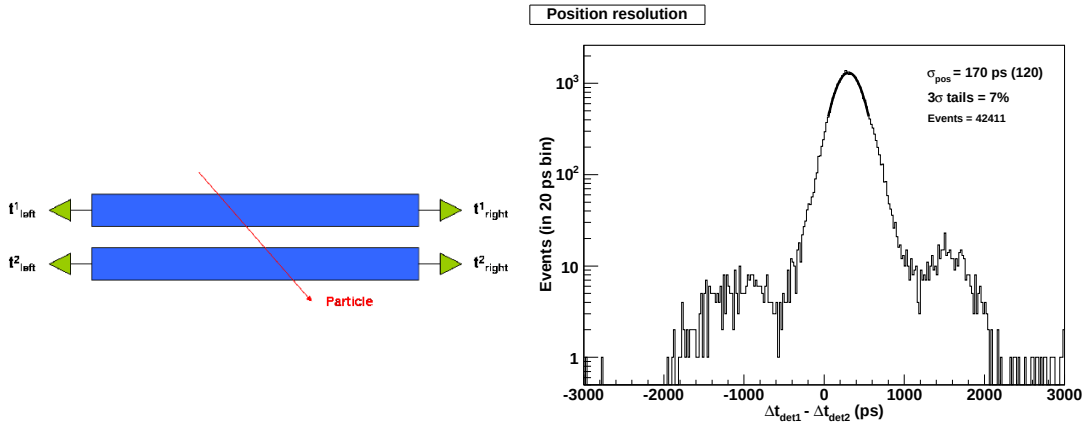


Figure 6.17: *Left: schematic of two overlapped cells for tof measurements. Right: tRPC position resolution distribution, showing a σ_{pos}=12 mm. The cell width is ∼2 ns. The big background comes from double hits.*

width of the cell. This background is attributed to double hits, and a probability of 1% of double hits was estimated.

6.5.5 Crosstalk measurements

The estimation of the crosstalk between cells can be done when several cells are instrumented and there are two overlapped (for example, detectors in the same layer). If a particle hits one detector, signals in a non-overlapped detector with the first one at the same time can be attributed to two factors: the electronic crosstalk or the double hit probability. It has been shown that an induced crosstalk signal can produce a valid timing signal in the FEE channel but without charge [22]. Since we have charge information through the ToT measurement, crosstalk signals can be discriminated from the valid hits easily. In this way, a probability below 1% for double hits was obtained, being consistent with the value estimated in section 6.5.4.

Two crosstalk estimations were performed by looking for signals without charge information. First, a crosstalk between cells was estimated when two different cells were connected to different DBOs. In this case, a crosstalk around 1% was measured, being compatible with previous measurements [64]. On the other hand, such measurement was also performed when the cells were connected to the same DBO obtaining the possible electronic crosstalk. For all thresholds, crosstalk values ranged from 2% to 6% depending on the DBO board analyzed.

6.5.6 Conclusions

In November 2005, a first prototype of the HADES tRPC detector instrumented with 24 cells together with the full electronic chain (DBO-STEP4 mainly, MBOv1 and TRBv1) was tested with beam at GSI (Darmstadt, Germany).

The time resolution of the full system was measured, providing 80 ps and 77 ps before and after the slewing correction, respectively. This correction applied with the ToT algorithm reduced the tails from 4.5% to 3%. The improvement in the time resolution was not significative because the ToT algorithm was not optimized and new improvements were needed: namely to increase the ToT range and to decrease its trailing edge jitter. The position resolution of the cells showed a mean value of $\sigma_{pos}\sim$12 mm integrated over the full cell, being dominated by the electronic jitter.

The probability of crosstalk between cells was also estimated. A detector crosstalk was estimated ∼1% and a possible electronic crosstalk was changing from 2% to 6%, depending on the board. A probability of double hits stayed below 1%.

6.6 Improvements in the STEP4 design

This work was developed at the GSI after the beam time done in Nov05, together with Dr. W. Koenig. The most important features of the FEE to be improved were:

- The stability of the FEE together with the rest of the system, RPC and DAQ.
- The behaviour of the ToT algorithm to measure the charge.
- The time resolution for small signals.

6.6.1 FEE stability

The FEE stability required some improvements in the layout, the hysteresis of the discriminator and the thresholds. During the beam time we discovered that one of the DBO channels was less stable, founding a mistake in the layout of the threshold line of that channel. The solution was to improve the grounding in the MURATA 4-paths capacitor existing before the discriminator. In order to improve the stability we also decreased the hysteresis value of the discriminator to the minimum (∼3 mV, see Fig. 4.13), increasing the resistor to ground of the hysteresis. Once these changes were implemented, an improvement in the FEE stability was obtained, being the channels completely stables for ToF thresholds above 5 mV (<100 μV_{RMS}). And no crosstalk effects were observed for threshold$_{ToF}$>3 mV.

Other important point regarding FEE stability was to improve the DBO-MBO connection. The connectors used for STEP3 and STEP4 boards were not optimal connected. So, the noise at the amplifier level was increased affecting to time measurements. Some structures in the ToT spectra were also found due to these connectors. For the final design it was necessary a better connector to avoid these noise effects. Different connectors from ERNI, KEL and SAMTEC were tested. The final choice was to fix the DBO and the MBO forming a 90° angle, using card edge connectors from the SAMTEC HSEC8 series (40-pins of 0.8 mm pitch), specific for high frequencies to preserve the transmitted signal (see chapter 7 and www.samtec.com).

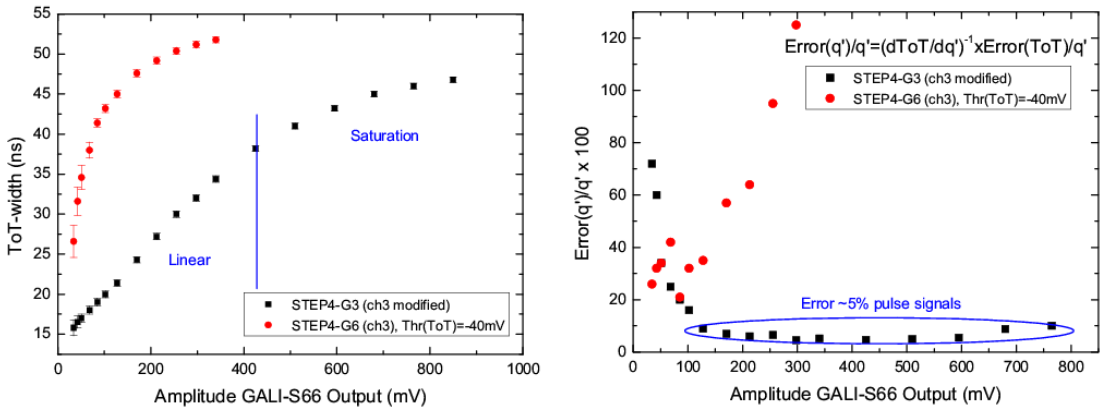


Figure 6.18: *Comparison between a modified channel with the new LE configuration and an original STEP4 channel. Left: ToT-width vs amplitude. Right: incertitude in the ToT measurements vs amplitude, both with test signals.*

The grounding of the DBO was also improved making two holes in the upper region to screw the board to the MBO (see chapter 7).

6.6.2 Time over Threshold algorithm

The improvements in the ToT-charge behaviour were focused in two ways, done increasing the input capacitors of the preamplifier, reducing the ionic tail of the RPC signals and avoiding its integration:

1. Increasing the ToT range in the linear region.
2. Reducing its trailing edge jitter.

Increase the ToT linear range

In order to increase the ToT-charge range we increase the gain of the op-amp, being the Philips BGM1013 the new choice (see chapter 7 for more details).

The most important improvement was to modify the latch enable design. Instead of the ToT discriminator, we connected the output of the integrator directly to the $\overline{LE}$ and the $\overline{Q}$ output through a capacitor. The LE is connected to an external voltage reference level to control its baseline and also to the Q output through a capacitor. In this way, one discriminator channel is enough for each channel reducing the number of MAX9601 needed to two per DBO instead of four (see schematics in Appendix B). This solution reduce both the price and the power consumption. The first prototype was implemented with the same 47 pF capacitor in both LE inputs (see symmetric design simulation in chapter 5). The output signal is closed when both LE and $\overline{LE}$ cross them, being the width of the output signal proportional to the integrated signal and the charge of the signals. This 'Charge to Width' (QtoW) algorithm is slightly different of the ToT algorithm (see more details in chapter 7).

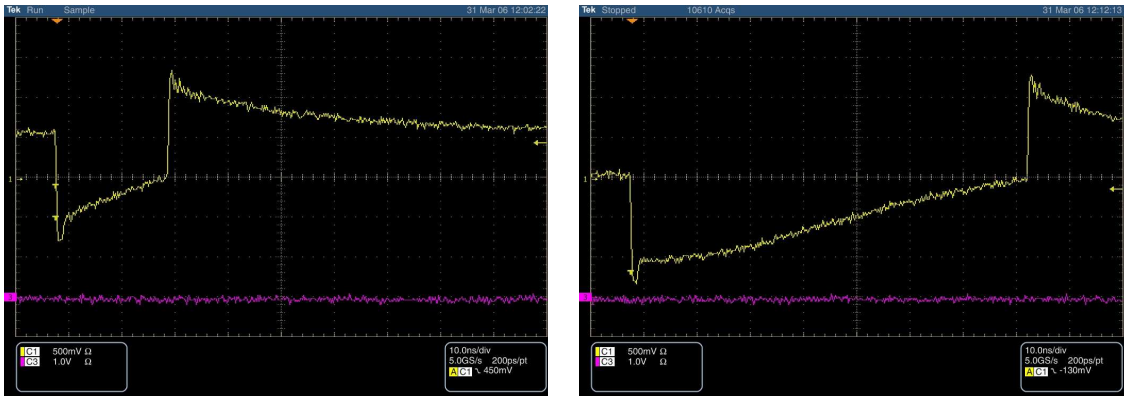


Figure 6.19: $\overline{LE}$ *behaviour for low (left) and high (right) ToT thresholds.*

Results with test signal are shown in Fig. 6.18. Both pictures present the comparison between an original DBO-STEP4 channel and a modified channel with this LE configuration. The left picture shows the behaviour of the ToT-width as function of the amplitude signal of the amplifier at both channels. With this new channel we increased the ToT-width range, getting a higher linear range required for the slewing correction. The insensitive width for large signals was still presented. This saturation effect is inherent to request low ToT thresholds. The right side shows the improvement in the error of the ToT-width measurements in this new design compared to the original one, concluding that the error in the ToT is <5% for typical signals, measured through the jitter of the trailing edge of the LVDS signal.

As was explained above, changing the ToT threshold it is possible to adjust the baseline of $\overline{LE}$ and the "linearity" behaviour of the ToT-charge (LE differentiation). Fig. 6.19 presents the different behaviour of the $\overline{LE}$ for a low ToT threshold value (left) and for a high value (right), showing the different baseline levels in each case.

Reduce the jitter of the trailing edge

Figure 6.20-right shows the jitter of the trailing edge of the LVDS output signals of two channels, giving both ∼100 ps. An average value of 130±50 ps was obtained with test signals, being a measurement of the QtoW algorithm error. Both measurements show a clear improvement respect previous designs.

6.6.3 Time resolution for small signals

In order to improve the time difference between two channels reducing the FEE time resolution for small signals, we analyzed time differences of the whole FEE chain (DBO+MBO+TRB). Improving the grounding between the boards, the noise-to-slope ratio could to be minimized, avoiding baseline oscillations and reducing the jitter. The test input of the DBO was also modified to inject small signals with an amplitude of ∼5 mV. The ToF threshold was set to 10 mV for each channel.

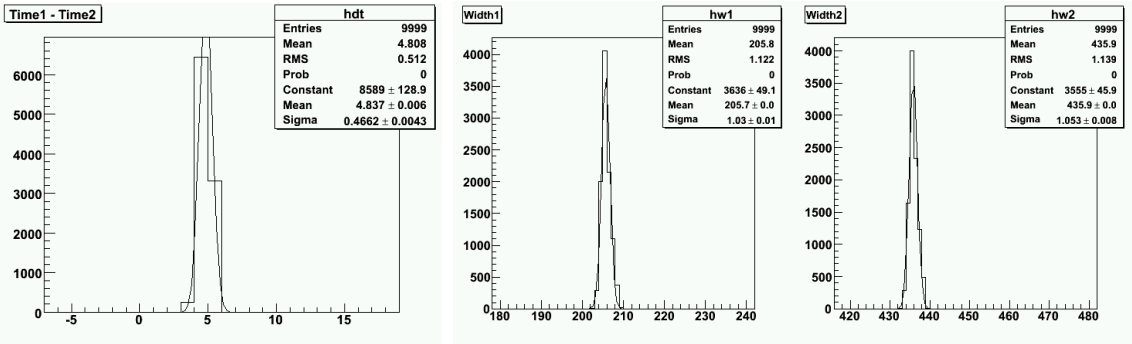


Figure 6.20: *Test signals analysis of a modified channel including the TRB-DAQ: time difference between two channels, showing a σ_T=46 ps combined for two channels (left) and the jitter of the trailing edge of two LVDS output signals, both providing ∼100 ps (right).*

Fig. 6.20-left shows the time difference between two channels for the whole chain FEE+DAQ, showing a σ_T=46 ps combined for two channels and 33 ps per channel. An average value σ_T=43±10 ps was measured, giving a σ_T=30 ps per channel measured with reference test signals. This σ_T is limited for the TRB acquisition board, being the TRB minimum resolution $\frac{100}{\sqrt{12}}$=28 ps per channel. As consequence we can conclude that the electronics will not limit the timing measurements of the RPCs.

6.6.4 Cosmic rays test

In order to evaluate the improvement in the ToT-width measurements done with test signals, a test with real RPC signals was needed. A cosmic ray test [11] was also done with the same prototype and FEE used in previous Nov05 beam-time. Two scintillating fiber detectors with a very good position resolution were placed over and below the RPC prototype. A dedicated analysis of the ToT and the charge signals was performed in an RPC cell that was instrumented with both FEEs (a new modified channel of our FEE with the new LE configuration and a reference channel from LIP), one in each end, allowing to have ToT and charge for the same event. Results are shown in Fig. 6.21.

The left picture shows the logarithmic ToT spectra. The fraction of streamers and high amplitude signals in the working point is <1%. There were also events giving signal in the reference channel but not in the new FEE. These low charge events represent a 5% of the total. Therefore, it seemed that the lower efficiency of the new FEE was due to an insufficient amplification for small charges. On the other hand, there were no events with signal in the new FEE and not in the reference one. Events with charge equal to zero are defined as events which gave a valid time signal (reference electronics fired), but no charge was registered in the ADC (attributed to a deficient configuration of the ADC).

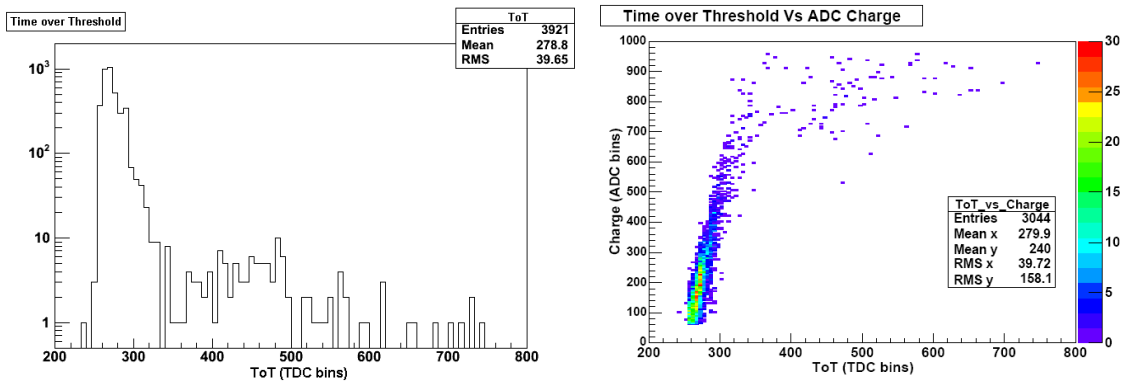


Figure 6.21: *ToT analysis with cosmic rays. Left: ToT-width spectra, showing <1% of streamers. Right: ToT as function of the charge. A linear behaviour is observed except for higher values, where the ToT saturates.*

Fig. 6.21-right shows the behaviour of the ToT as function of the charge measured. A linear behaviour of the ToT is observed, except for the higher charges, where the ToT value saturates. This linear behaviour was improved respect previous design, although the big dispersion in the ToT values for big avalanches and streamers was a problem and more tests were required.

6.7 FEE-STEP3 and STEP4 conclusions

Both designs FEE-STEP3 and STEP4 with the new DBO+MBO configuration were presented in this chapter. Several tests were performed, showing overall satisfactory results, although some improvements were needed.

A beam time test with this FEE and a prototype with 24 RPC cells took place, featuring good time resolutions (a σ_T=16 and 77 ps per channel was obtained for the FEE and the whole system, respectively).

The FEE stability and the behaviour of the new QtoW algorithm required some improvements in a new design:

- At the DBO side, some improvements for stability reasons (a better layout and a new DBO-MBO connector to screw both boards), in the ToT algorithm (reducing the number of discriminators with the new LE configuration).
- At the MBO side, an improvement in the test signal input and in the trigger summing stage of individual MBOs.

Chapter 7

DBO-STEP5 version: design, analysis and results

7.1 Introduction

In this chapter, we describe the so-called DBO-STEP5 and MBOv2 developed for the HADES timing RPC wall. As was mentioned in chapter 5, the FEE consists of two boards and a third one for the data acquisition [56], [89] (see Fig. 6.1):

1. A 4-channel DaughterBOard (DBO) using a fast 1-2 GHz amplifier feeding a dual discriminator with a constant threshold and an operational amplifier for a charge measurement by a 'Charge to Width' algorithm, that will be referred as QtoW [56], through the integrated signal.
2. A 32-channel MotherBOard (MBO) housing up to 8 DBOs and providing them voltage regulation, thresholds via DACs, test signals and a trigger logic. The MBO delivers the differential output signals to an external HPTDC chip [58], placed in the acquisition board.
3. A 128-channel TDC Readout Board (TRB) for the acquisition system [86].

7.2 The active board: the DaughterBOard STEP5

Next sections show the DBO-STEP5 [56] and the MBOv2 [88], [89] designs. The main differences in comparison with previous designs are:

- The new LE configuration (see section 6.6), providing the charge through the 'Charge to Width' algorithm (QtoW).
- The power consumption was decreased to 500 mW/channel, due to only two discriminators per DBO were required instead of four (see Appendix B).
- New MBO-DBO connectors to improve the stability of the FEE system.

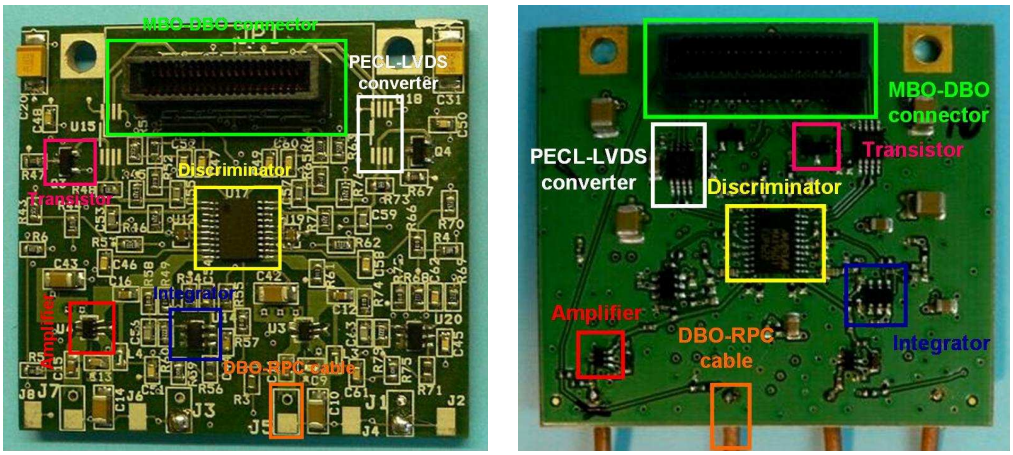


Figure 7.1: *Both 4-channel DBO-STEP5 board developed at the USC (left) and at the GSI (right) with 0603 and 0402 components, respectively (size 5×4.5 cm^2).*

The DBO-STEP5 is a 4-channel and 6-layer board, which size is $\simeq$5×4.5=22.5 cm^2. Figure 7.1 shows both boards of the same design, but with different layout, developed at the LabCAF-USC, the so-called STEP5.1, and at the GSI, the so-called STEP5.2. For the STEP5.1 we developed two boards: i) with 0603 passive components and ii) with 0402 components for having more free space in the DBO. The second version was chosen to develop the STEP5.2 board with the help of Dr. W. Koenig at GSI to compare them. The board showing better features was chosen.

There are two different channels in each side of the board, two on the TOP layer and two on the BOTTOM one. The connection between the DBO and the RPC was done through a RF connector series MMCX (see www.buerklin.com), type Telegärtner J0134. On the detector side one-channel, the female connector is mounted directly on the PCB. The male connector is fixed to a few cms long coaxial cable soldered directly to the input of the DBO, the RG405U 50 Ω Semi-rigid Coaxial Cables from Pro-Power (2.2 mm of nominal outside diameter).

In the design of the STEP5 board (see Appendix B) some technical issues were needed. In order to control the impedance of the paths as function of its width, thickness and the dielectric constant ε_r (specially in the analog part), we used the TXLine programm. For impedance matching in PCB traces [90] (see Fig. 6.3), the stripline solution was chosen because Equations 6.3 and 6.4 give higher impedance than the other ones (see section 6.2). This is an advantage also for EMI protection, because ground and/or power planes can be placed on the outer layers. Distance between traces should be as large as possible to maximize the impedance. We must also connect to ground several points of the board using vias to minimize the parasitic inductances and put coupling capacitors to ground as close as possible to the amplifier. And we must center the holes of vias to avoid possible noise effects.

The block diagram of the DBO-STEP5 is shown in Fig 7.2, where the part inside the box corresponds to the DBO, showing the analog and the digital stages (see the

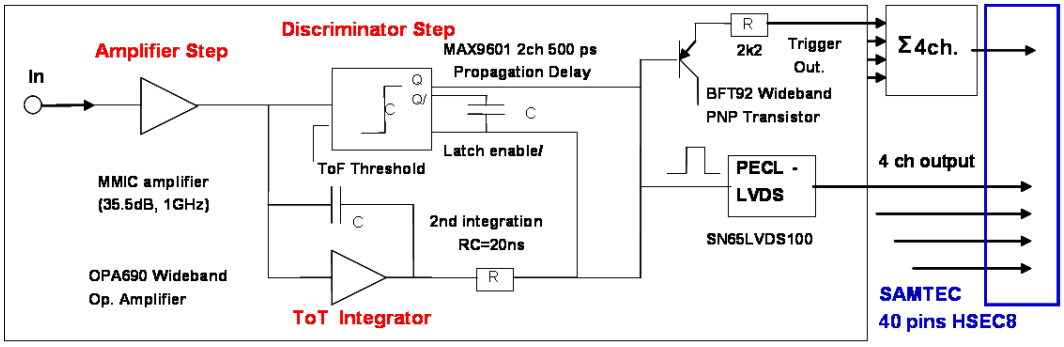


Figure 7.2: *Simplified DBO-STEP5 block diagram, showing all the important steps: amplification, integration and discrimination.*

schematics and the layout in Appendix B). The main features of the STEP5 are:

1. One amplification stage with a factor of amplification $G{\sim}40$.
2. One LVDS digital output signal to measure the time information and the charge through the 'Charge to Width' (QtoW) algorithm.

7.2.1 Analog stage

The analog part of the STEP5 was also based in a MMIC amplifier following previous works [28], [47] since the input signal has frequency components extending up to the GHz range. The amplifier chosen was the Philips BGM1013 featuring 35.5 dB power gain at 1 GHz (31 dB flat gain up to 2.2 GHz), 4.5 dB noise figure at 1 GHz and high linearity, providing a high gain-bandwidth product (GBW$>10^{11}$). This amplifier works with an impedance of 50 Ω, which has proven to be quite convenient, allowing the input connection to be made through a standard cable and being sufficiently low to reasonably match the 20 Ω detector impedance [78].

The BGM1013 amplifier was also split in two parallel branches with the same components of previous version (see chapter 5): (a) one goes to an integration stage using the TI OPA690, a wideband operational amplifier, and (b) another one goes to the dual Maxim ECL/PECL MAX9601 ultrahigh speed discriminator, where it starts the digital part of the design (Fig. 7.2). This integrated signal is used for the charge measurements through the 'Charge to Width' (QtoW) algorithm [56], where the width of the LVDS output signal is proportional to the RPC signal charge.

7.2.2 Digital stage

The digital stage of the DBO-STEP5 starts with the same dual ECL/PECL MAX9601 discriminator (Fig. 7.2). The main difference respect the STEP4 design is each of these discriminators are shared between two channels due to the new LE configuration. Then, only two discriminators are needed: the amplifier outputs of

GND	1	2	GND
ToF/ToT B high	3	4	ToF/ToT A high
ToF/ToT B low	5	6	ToF/ToT A low
GND	7	8	GND
+5 V	9	10	-5 V
+5 V	11	12	-5 V
Test Signal A/B	13	14	-5 V
GND	15	16	Threshold ToF A
Threshold ToF B	17	18	Threshold ToT A
Threshold ToT B	19	20	Threshold ToF C
Threshold ToF D	21	22	Threshold ToT C
Threshold ToT D	23	24	GND
GND	25	26	Multiplicity-4
Test Signal C/D	27	28	GND
+3.3 V	29	30	+5 V
+3.3 V	31	32	+5 V
GND	33	34	GND
ToF/ToT D high	35	36	ToF/ToT C high
ToF/ToT D low	37	38	ToF/ToT C low
GND	39	40	GND

Table 7.1: *Pin-out assignment for the MBOv2 and DBO-STEP5 connector.*

two channels go to one dual MAX9601 for the time information (ToF discriminator with a positive threshold level). As we have a positive ToF threshold and the amplifier is non-inverting, positive RPC signals are required in the detector.

Latch Enable configuration

The latch enable of the discriminator provides the trailing edge of the digital signal when both signals cross each other. $\overline{LE}$ and LE are connected to the integrated signal and to an external DC level, respectively (see section 6.6). With the external DC level we can change the LE baseline and control the output width. In the STEP5 board both latch enable inputs are symmetric: the output of the integrator is connected to the $\overline{LE}$ through a R=1 kΩ and the $\overline{LE}$ is connected to the output $\overline{Q}$ of the discriminator through a C=20 pF, producing the discharge of the $\overline{Q}$ [56]. In this way, the digital pulse encodes both the timing and the charge of the RPC pulses. The leading edge is used for the time of flight measurements and the charge-width is used for calibration purposes.

A TI SN65LVDS100 PECL to LVDS converter provides the LVDS signal required by the DAQ system. The DBO provides also a multiplicity signal needed to the HADES trigger unit through a summing step of the 4 channels in each DBO (done with the same BFT92 transistor), which is sum again in the MBO.

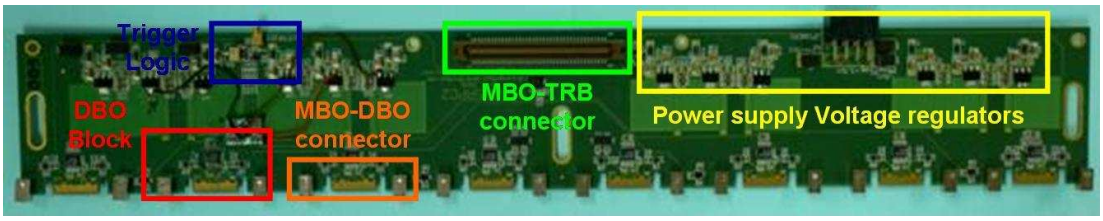


Figure 7.3: *Top view of the MBOv2, housing 8×4 channels (size 40×6=240 cm^2).*

DBO-MBO connector

In the previous designs, after connecting the DBO to the MBO a few times the connector became unstable and some pins did not make a good contact. For avoiding this effect, in this design we selected a card edge connector from the SAMTEC HSEC8 series (see www.samtec.com). The connector, placed only in the DBO side, fits into plated pads located at the edge of the MBO (Figs. 7.1 and 7.3), featuring 40 pins of 0.8 mm pitch, specified at high frequency (up to 8 GHz) to preserve the transmitted signal. The DBO is still screwed to the MBO for more stability.

The pin-out assignment criteria is the same as in the previous version, but some pin redistribution was done to readapt the new number of pins (Table 7.1).

7.3 The passive board: the MotherBOard MBOv2

The MBO is the interface between the DBO and the TRB and provides:

- Stable and low ripple power supply voltage and ground.
- Programmable thresholds controllable via DACs.
- Test input signals and paths for the readout of all the detector signals, trigger signals and temperature sensors.

The MBOv2.0 (Fig. 7.3) was developed by A. Gil at IFIC, being an upgrade of the previous design [80], [89] with 32 channels and the same size. The 32nd channel is used to have the reference time needed by the acquisition. Due to space restrictions, a short version of the MBO for three DBOs (12 channels in 16.5×6.5 cm^2) has been made to instrument the wider part of the wall. The MBO-TRB connector is the same KEL8930 series with 80 pins used in the MBOv1. The pin-out group all differential signals on one side (see Fig. 12, Appendix B), providing also interface for the SPI communication, both test signals delivery and the temperature sensor.

Some improvements were done in the MBOv2 respect to the MBOv1 presented in chapter 6. A read-back DAC feature was included to verify the correct programming of the thresholds. The test signal scheme is now controlled from the TRB to avoid manual channels selection. The supply filter was redesigned to improve regulation

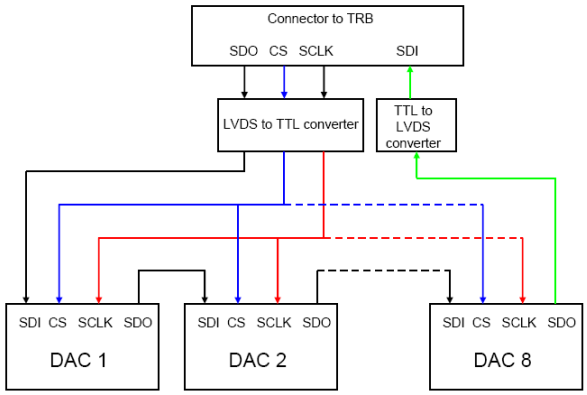


Figure 7.4: *Daisy-chain configuration for the DAC with 'read-back' implemented.*

at low frequencies and to provide better noise rejection. A temperature sensor for monitoring was also included. New holes were added at the center and at the edges of the MBOv2 to screw it to the RPC box for improving the grounding (Fig. 7.3).

7.3.1 DAC read-back

A basic read-back was required to verify the correct programming of the DAC thresholds and to detect failures in the DAC chain. A few DACs on the market incorporate read-back feature, checking the voltages programmed at the output by reading the last value stored in the internal registers. Nevertheless, they have some disadvantages respect to the original LTC2620: large package (64 pins) and more consumption and output noise. We decided to keep the LTC2620 (12 bit resolution, low power consumption and very low output noise) to set the thresholds and to include a basic read-back feature that can be implemented taking advantage of the internal shift registers by reading the content of the register after it was written.

Negative thresholds needed to adjust the LE baseline are obtained by using 8-channel operational amplifiers in inverting configuration. Eight DACs installed in the MBO are daisy chained and can be programmed using the same control lines by SPI used for setting the thresholds.

In order to verify the correct programming of the DAC and to simplify the FEE, the checking was limited to read the content of the shift register of the DAC after every programming operation. This is easily done by clocking out the data stored in the register and comparing it with the programming data sent for setting thresholds.

Figure 7.4 shows the TTL to LVDS converter needed to transmit the internal register value back to the TRB. As low noise levels at each channel output do not guarantee low noise levels on MBO side because noise can be coupled to the signal trace, the noise level of the threshold voltages was reduced by increasing the V_{REF} pin of the LTC2620 from +3.3 V to +5 V and putting a resistor divider as close as possible of the discriminator of the DBO to reduce the noise by a given factor.

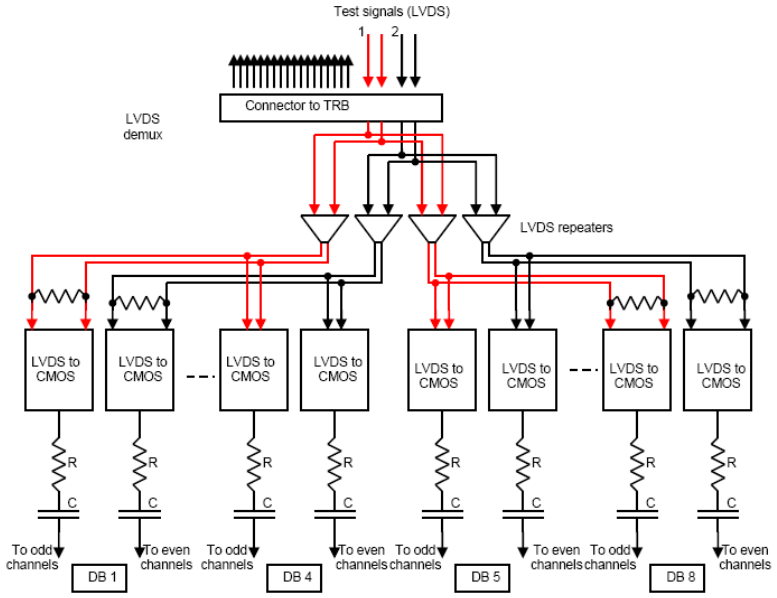


Figure 7.5: *Scheme of the test signals transmission from the TRB to the DBO.*

7.3.2 Test signals

Test signals are used to check the channels. The delivery system of the test signals in the MBOv1 was done by a manual switch placed on the board. The new version can do this task remotely by using the block diagram shown in Fig. 7.5. Two test signals can be sent from the TRB instead of one to odd and even channels or to all channels. Four SN65LVDS100 drivers, that replace the differential de-multiplexer MAX9169 of the MBOv1, deliver the LVDS signals to eight CMOS converters and a passive RC differentiator generates the narrow test signals (as in MBOv1). A large test signal of large amplitude is sent to the DBO to reduce noise injection in the test inputs. A larger divider factor on the DBO provides a larger noise reduction.

7.3.3 Supply voltage improvements

Voltage regulators

The test performed for the MBOv1 showed the need of improving voltage stability, including voltage regulators. This provides regulation and stability in case of using long power cables and reduces the noise associated with power switching supplies, producing a good rejection at low frequencies and some rejection at higher ones.

Three types of linear voltage regulators are available in the market [103]:

1. Standard (NPN Darlington) regulator.
2. Low Dropout regulator (LDO).
3. Quasi LDO regulator.

The most important difference between them is the dropout voltage, defined as the minimum voltage drop required across the regulator to maintain the output voltage. The LDO regulator requires the least voltage across it, while the standard one requires the most. Other important difference is the ground pin current required by the regulator when driving rated load current. The standard regulator has the lowest ground pin current, while the LDO has the highest.

In order to stabilize the gain of the preamplifier we chose the LDO regulators [55] because their reduced voltage drop minimizes the heat released. The pass device of the LDO regulator is made up of a single PNP transistor. Then, the minimum voltage drop required across the LDO regulator to keep regulation is the voltage across the PNP transistor (VCE). Thus, features considered for the selection of the voltage regulators were:

- Small voltage drop to reduce the power consumption and heating and high ripple/noise rejection to provide additional ripple and noise reduction respect to the obtained by capacitors for switching power supplies.
- Compatibility with low ESR output capacitor. Regulators with tantalum capacitors (large ESR) are not optimal for noise reduction at high frequencies.
- Over-current and thermal shutdown.

The new power supply filtering was done by taking as reference the power consumption of the DBO measured in the laboratory: 330 mA for +5 V, 160 mA for +3.3 V and 150 mA for -5 V. The LDO selected are the ADP3338ACK (for +5 V and +3.3 V) from Analog Devices, and the LT1175 (for -5 V) from Linear Technology.

The ADP3338 has a typical drop voltage of 190 mV at full load and a maximum output current of 1 A, being short-circuit protected by limiting the drive current in the transistor base to 2 A. Since a DBO only requires the third part, every LDO feeds two DBOs, leaving enough current safety margin. Its stability depends on the output capacitor. The ADP3338 is protected against power dissipation damages by its thermal overload protection circuit, being the maximum temperature 160 °C. Current and thermal limit protections protect it against overload conditions.

Negative regulators have worse features than the positive ones. Thus, for a maximum output current of 0.5 A, the LT1175 produces a typical voltage drop of 350 mV. These LDO can also operate without restrictions in the ESR output capacitor. Package ST (SOT-223) was chosen for all the regulators in order to take advantage of the better thermal resistance provided by this package respect to the DIP one.

Power ripple filtering scheme

As the FEE is powered by a switching power supply, special care was taken in the design of a power ripple filtering scheme [80], [89]. Regulators provide an excellent ripple/noise filtering at low and medium frequencies but not at higher ones. Thus,

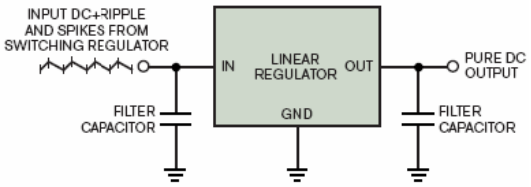


Figure 7.6: *A conceptual linear regulator and its filter capacitors theoretically reject switching-regulator ripple and spikes.*

some additional components for high frequency filtering become mandatory when an LDO is powered by a switching regulator, because it must be able to cope with switching frequencies beyond 300 kHz. All linear regulators have some difficulties to reject ripple and spikes, especially at high frequencies [104]. These effects are unfortunate because small voltage drop is desirable for maintaining efficiency. Input-filter capacitors smooth the ripple and spikes. The output capacitor keeps low output impedance at higher frequencies, and improves load transient response.

Fig. 7.6 shows the dynamic AC-output content of a switching regulator. It comprises low-frequency ripple at the switching regulator clock frequency and high-frequency spikes. The switching regulator pulsed energy creates the ripple. Filter capacitors smooth it but do not eliminate the AC content. Regulators reject better ripple than wide-band spikes. Power Supply Rejection Ratio (PSRR) is a measure of how well the regulator rejects an AC signal riding on a nominal input DC voltage:

$$PSRR(dB) = 20 \times \log \frac{\Delta V_{OUT}}{\Delta V_{IN}} \tag{7.1}$$

The power-supply rejection ratio is maximum at low frequencies and begins to fall from 1 kHz to 100 kHz, depending upon the regulator design. Some methods can improve the PSRR of the regulator [105] and we choose to put ferrite beds.

A ferrite bead enclosing a conductor provides the highly desirable increase of the impedance as frequency rises. This effect suits high-frequency noise filtering of conductors carrying DC and low frequency signals. At higher frequencies, the bead ferrite material interacts with the conductor magnetic field creating the characteristic loss. It is possible to reduce spikes to <1 mV by adding ferrite filtering at the input/output of the regulator [106]. A BLM41PG102SN1 from Murata is included at the input, providing an impedance of 1 kΩ at 100 MHz, and a BLM18PG121SN1 with less impedance but better DC impedance (0.05 Ω) is placed at the output.

7.3.4 Trigger output signal

The trigger system provides information about the number of channels fired in each event. The MBO collects the trigger signals from the 32 channels and generates a trigger output signal (see Tables 5.3 and 5.4 for voltage levels). The trigger output

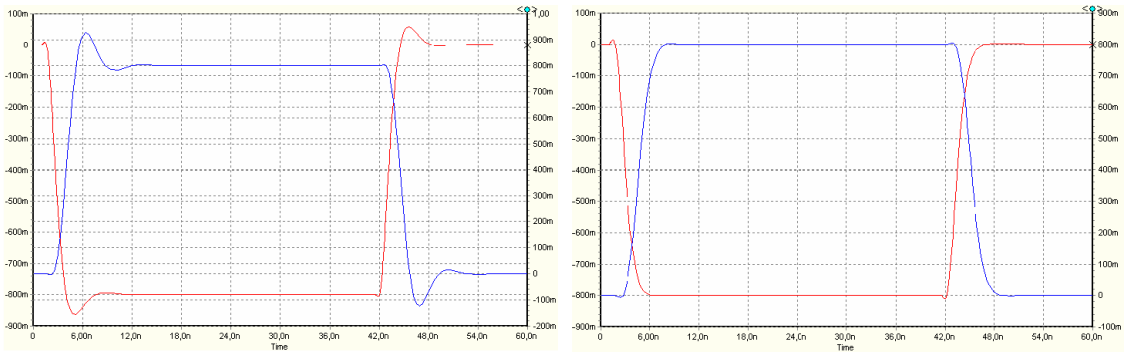


Figure 7.7: *Overshoot analysis with a 0.2 (left) and 1.2 pF (right) feedback capacitor in the output trigger signal.*

LEMO connector used in the MBOv1 was replaced by the new MMCX type (similar to the DBO-RPC connector) for some space saving (Fig. 7.3).

OPA690 was a good candidate for the low level trigger implementation mainly because of its high slew rate (1800 V/μs) and high output swing ($\pm$4 V), but provides a big overshoot (>15%, see Fig. 7.7-left). This overshoot gets values bigger than 100 mV for medium and large signals, being an inconvenience because it can indicate a wrong number of fired channels. This problem get worse using several amplifiers in cascade, as was noticed during the Nov05 beam time. The solution chosen was to reduce the bandwidth of the OPA690 by a small feedback capacitor. According to a simulation (Fig. 7.7-right), a 1.2 pF capacitor almost eliminates the overshoot.

7.3.5 Temperature sensor

An increase of the temperature may be a warning on the system. To prevent failures, a temperature sensor was included on the MBO. Originally, SPI temperature sensors were considered to take advantage of the SPI protocol already implemented, discarding them due to the impossibility of including the sensor into the DAC chain.

The temperature sensor DS18B20 was used, a digital thermometer featuring $\pm$0.5 °C accuracy over a -10 °C to +85 °C range, being independent of the SPI. It offers thermostatic functionality with over-temperature (TH) and under-temperature (TL) programmable set points, stored in on-chip EEPROM[1]. An internal flag is set when the temperature is higher than TH or lower than TL. If thermostatic operation is not required, both TH and TL bytes may be used for general-purpose non-volatile storage (i.e., MBO identification). Its main features are the following:

- Temperatures measurement from -55 °C to +125 °C (-67 °F to +257 °F). It converts temperature to 12-bit digital word in a maximum of 750 ms.
- Data is read out over 1-Wire serial bus interface with programmable 9 to 12-bit user-configurable resolution and 3.0 V to 5.5 V supply range.

[1]Electrically-Erasable Programmable Read-Only Memory.

- Only one port pin for communication is required on the MBO-TRB connector.
- 64-bit unique and unchangeable electronic serial number.
- Alarm function and no external components are required to sense temperature.

7.4 Test of the two FEE versions

In this section, some results of the analysis done on the data taken at January 2007 test in the GSI are presented. The main aim of this test was to analyze the behaviour of the the two different STEP5 boards developed with the same design but having a different layouts (see section 7.2): STEP5.1 (USC) and STEP5.2 (GSI).

7.4.1 Experimental setup

The experimental setup consisted on the same RPC prototype box (Fig. 6.13) of the previous Nov05 test (see section 6.5) with 24 cells, two DBO-STEP5 boards, the MBOv2 and the TRBv1. A plastic fast scintillator was used as external cosmic rays trigger (1-2 Hz) and placed in front of the gas box, covering partially the active area of some cells. This external trigger goes to a discriminator and then to the TRB. For test signals we used the multiplicity trigger provided by the FEE.

Two kind of measurements were developed:

1. With test signals injected in the FEE through the TRB.
2. With real RPC cells signals injected directly to the DBO.

7.4.2 Test signals analysis

Some results of both boards are presented with and without detectors connected to DBO channels, analyzing the time resolution and the jitter of the QtoW signal.

Test signals analysis without RPC

We equipped one MBOv2 with five DBOs and the test signal coming through the TRBv1 was sent to all even and odd channels. The trigger signal required by the TRB was the multiplicity trigger signal provided by each DBO and generated through the MBO. Figure 7.8 shows the time difference between two DBO channels with test signal coming from TRB and the jitter of the QtoW width.

Regarding the time difference measurements, the σ of the distribution is the time resolution combined for two channels. Results for both DBOs are similar, giving a σ_T <40 ps/channel, 55 ps combined for two channels (Fig. 7.8-left). About the jitter of the width of the LVDS output signals (QtoW), results are similar for both designs.

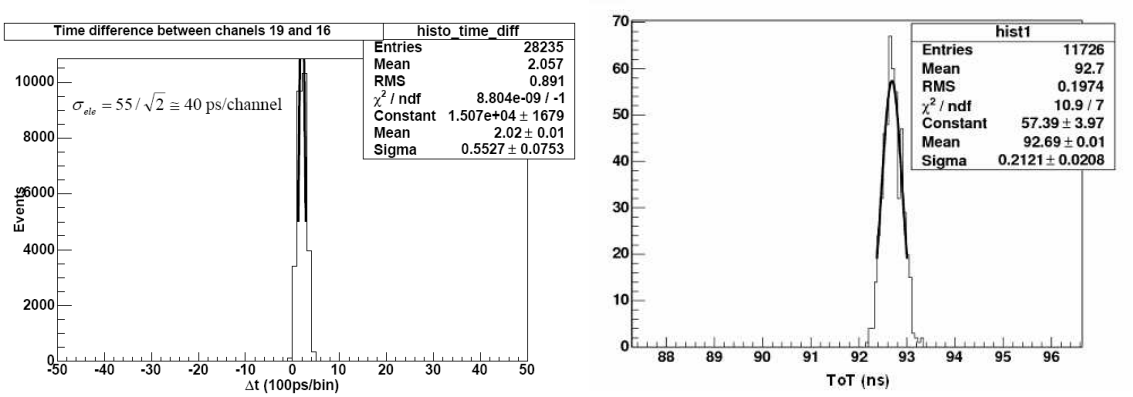


Figure 7.8: *Test signals analysis of the DBO-STEP5.2. Left: time resolution between two channels, showing a σ_T <40 ps/channel. Right: jitter of the QtoW, showing a value of ∼200 ps.*

It varies between 130 ps and 250 ps, giving a mean value of ∼200 ps (Fig. 7.8-right). Both tests do not show differences between both DBO designs, but the stability is higher for the DBO-STEP5.2. Due to this difference, the ToF thresholds are lower for this version. In both cases, the ToT threshold were set to 0 mV, and the ToF thresholds were set to 40 mV and 25 mV for STEP5.1 and STEP5.2, respectively.

Test signals analysis with RPC connected

Fig. 7.9 shows the results of the same measurements presented in Fig. 7.8, being now the DBO channels connected to the RPC cells. In this setup we equipped one MBOv2 with two DBOs, one of each design, connected to both sides of the same cell. The multiplicity trigger signal was generated by each DBO and distributed by each MBO to the same TRB. Thresholds are the same explained above.

The time difference between two channels show similar results for the time resolution of both designs, $\sigma_T \simeq 70$ ps/channel. This result is worst than the one when the RPC cell was not connected. The main difference are the bigger tails in the STEP5.1, indicating that the ToF threshold is much closer to the noise level and showing a less stable behaviour. Regarding the QtoW jitter, results are similar to the previous case, showing a jitter of the trailing edge of the LVDS signal ∼200 ps.

7.4.3 RPC signals analysis

Data were taken with cosmic rays through five days. The RPC box was equipped with two DBOs (one STEP5.1 and one STEP5.2) connected to a different MBOv2. The external trigger signal for the TRB was provided by a fast plastic scintillator covering some overlapped cells (see Table 7.2, also shown the corresponding electronic channels). The HV was set to 5.6 kV and the thresholds are the same than in previous section. The dark rate was ∼0.1-1 KHz and the dark current was 15-50 nA.

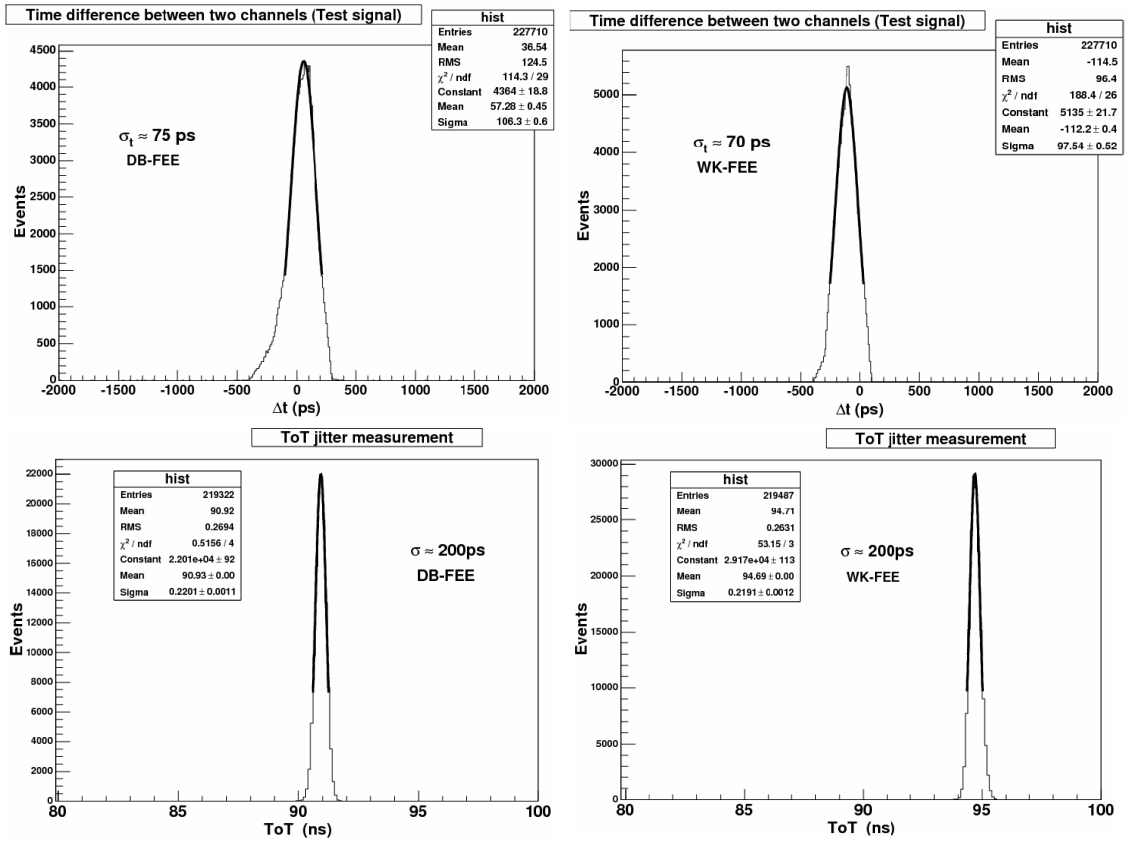


Figure 7.9: *Test signals analysis of DBOs connected to the RPC. Left: for the USC-DBO. Right: for the GSI-DBO, showing a time difference between two channels $\sigma_T \simeq$70 ps/channel (with more tails in the USC design) and a jitter of the QtoW $\simeq$200 ps in both cases.*

Table 7.2: *Correspondence between RPC cells and FEE channels.*

Cell	Left B detector	Right B detector	Left F detector	Right F detector	Cell
BC11[a]	USC6-ch4	USC8-ch2	USC6-ch3	USC8-ch1	FC9[b]
BC9	USC6-ch2	USC8-ch4	USC6-ch1	USC8-ch3	FC7
BC5	GSI1-ch4	GSI3-ch2	GSI1-ch3	GSI3-ch1	FC3
BC3	GSI1-ch2	GSI3-ch4	GSI1-ch1	GSI3-ch3	FC1

[a] Cells of the back layer, being all in the central row.
[b] Cells of the front layer, being all in the central row.

We imposed the overlapping condition between cells. Detector pairs BC11-FC9 and BC9-FC7 were instrumented with DBOs developed at USC and the remaining pairs, BC5-FC3 and BC3-FC1, with DBOs developed at GSI. The gain in these last boards was different because they implemented two amplifiers, one used a Philips BGA2712 (the same than in previous designs) with a gain of $G\sim$10 and the other used a Philips BGM1013, the same used by the USC boards with a gain of $G\sim$40.

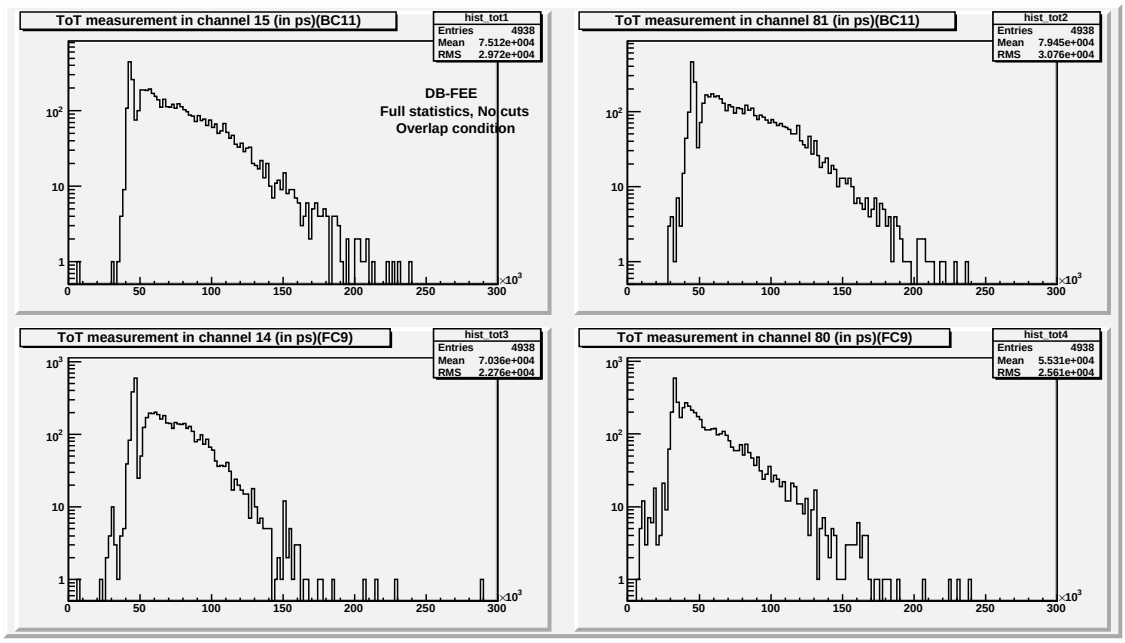


Figure 7.10: *QtoW spectrum for BC11 and FC9 overlapped cells using STEP5.1.*

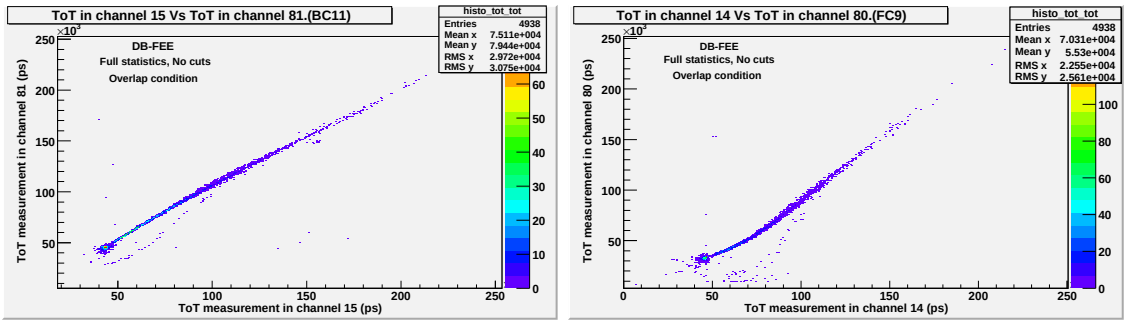


Figure 7.11: *QtoW measurements at both sides of BC11 and FC9 cells using STEP5.1 boards.*

Detectors BC11-FC9

The analysis have been done looking at the QtoW spectrums, QtoW vs QtoW, the time difference between both RPC sides, the time resolution with and without slewing correction and the time resolution over time. The analysis of these cells were done setting the ToF thresholds to 40 mV. Figures 7.10 and 7.11 shows the QtoW spectrums (in the plots is written ToT) for both sides of each cell and QtoW vs the QtoW plot for both sides of the same cell.

The QtoW spectrum of the BC11 cell is quite similar at both sides of the cell (Fig. 7.10). The streamers region is not clear because of the low statistics, but there is a small bump for bigger signals. The QtoW measured at both sides of the cell shows an approximate linear behaviour (Fig. 7.11), as was expected; both sides of

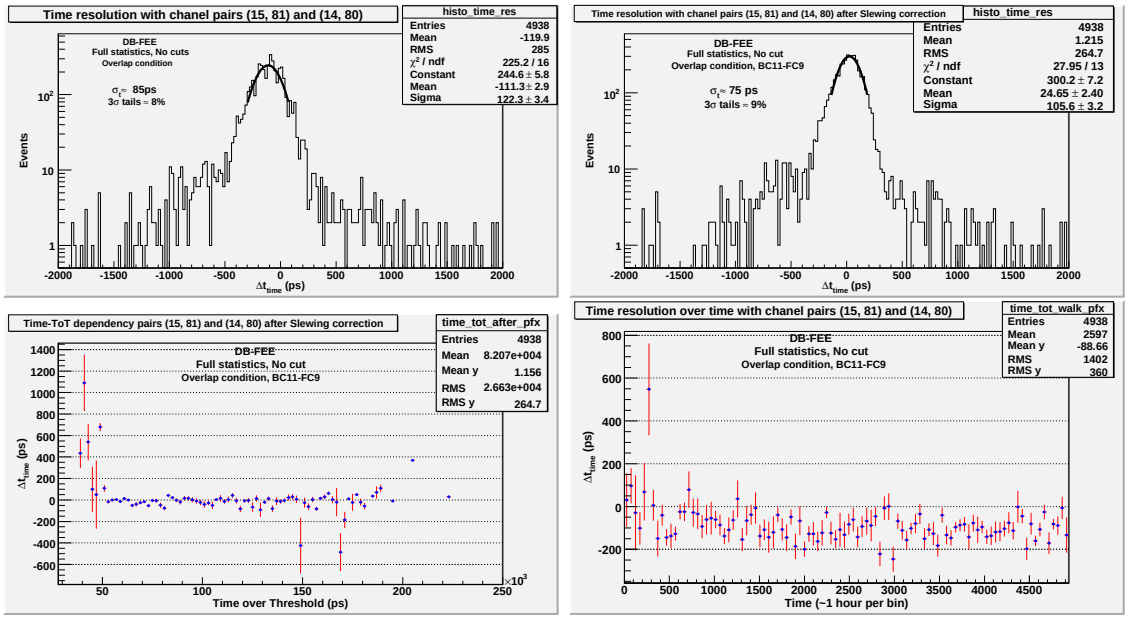


Figure 7.12: *Up: time resolution measured with BC11 and FC9 overlapped cells, before and after apply the slewing correction. Down: relation between time and QtoW after the slewing correction (left) and time resolution over the time (right).*

the same cell measure the same charge spectrum. The QtoW spectrum of the FC9 cell is slightly different at both sides, explaining the odd behaviour observed at low charges in QtoW vs QtoW plot (it is not linear). Peaks at ∼50 ns correspond to zero charge signals. A few events in Fig. 7.12 show an odd behaviour, probably caused by a malfunction of one of the channels.

Figure 7.12 shows the time resolution before and after apply the slewing correction, together with the Δt as function of the QtoW after apply the correction. To measure the time resolution two overlapped detectors are needed. The time of flight of a cosmic particle between both cells is measured by Eq. 6.10 (Fig. 6.17-left). For a $v \simeq c$ particle impinging perpendicularly Δt should be constant and the width of the $\frac{\Delta t}{\sqrt{2}}$ distribution provides the time resolution of a single detector. Last plot shows the behaviour of the time resolution along the time. No significant effects are visible during a long period of time. The time resolution before and after applying the slewing correction are 85 and 75 ps/channel, with around 8% and 9% of 3σ tails.

Some of the signals of the previous analysis were odd signals either due to crosstalk effects or noise. We may reject most of them doing a cut in QtoW>50 ns (approximate value of the QtoW output for zero charge signals). With such a cut most of the crosstalk events and tails are rejected (see Figures 7.13 and 7.14). Fig. 7.13 shows how the time resolution improves smoothly and the number of tails decrease significantly (1.5% 3σ tails). Fig. 7.14 shows the QtoW spectrums at both sides of each cell, providing better profiles than without cuts, specially for lower charges.

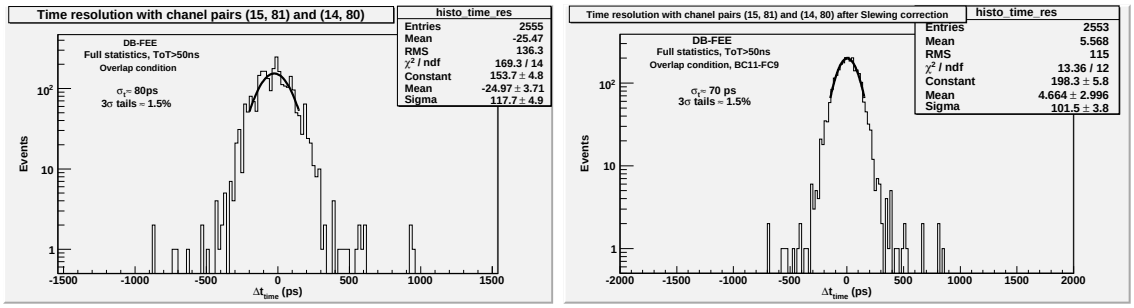


Figure 7.13: *Time resolution with QtoW>50 ns cuts using STEP5.1 boards.*

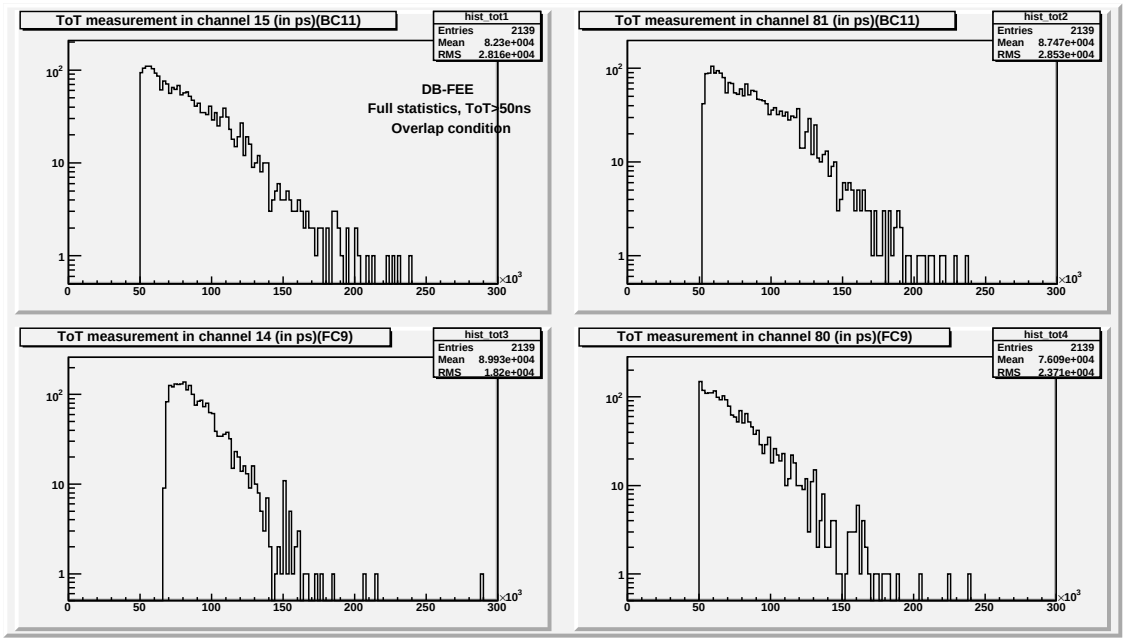


Figure 7.14: *QtoW spectrums applying a cut for QtoW>50 ns on BC11 and FC9 overlapped cells using DBOs-STEP5.1.*

Fig. 7.15 shows the position resolution in these cells, before and after applying the QtoW cut. In both cases it is around 8 mm, but the cut reduced the tails from 9% 3σ to 1.5% 3σ. The improvement in the number of tails is clear in all measurements (position, time and QtoW profile).

The position of a cosmic particle between two overlapped detectors is given by:

$$\Delta t_{pos} = (t^1_{left} - t^1_{right}) - (t^2_{left} - t^2_{right}) \tag{7.2}$$

where right and left are the both sides of the same cell (see Fig. 6.17-left). Assuming that incertitude in both differences are due only to the electronics, the incertitude in the position may be written as:

$$\sigma(\Delta t_{pos}) \cong 2\sigma_T|_{electronics} \tag{7.3}$$

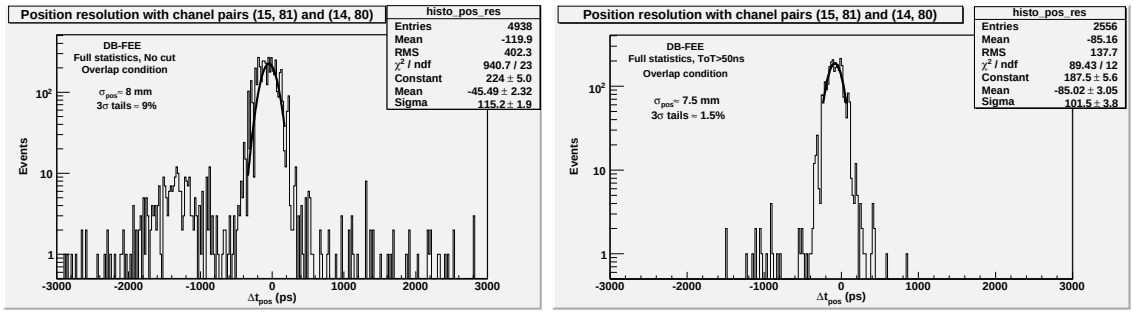


Figure 7.15: *Position resolution full statistics (left) and with QtoW>50 ns cuts (right) for STEP5.1 boards, corresponding to the BC11 and FC9 cells.*

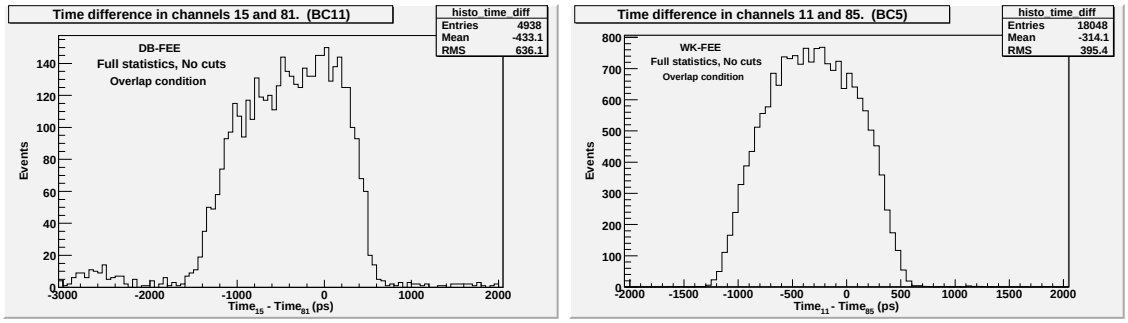


Figure 7.16: *Time difference between both sides of the BC11 cell (left), instrumented with a STEP5.1, and BC5 cell (right), instrumented with a STEP5.2.*

Detectors BC5-FC3

Overlapping detectors BC5 and FC3, instrumented with two STEP5.2 boards, were used to compare both STEP5 designs respect the previous analysis. An important point regarding the STEP5.2 boards used in this analysis is the different amplifiers implemented in each board, with different gain factors: a Philips BGA2712 with a gain of a factor $G\sim10$ and a Philips BGM1013 with a gain $G\sim40$. In this setup, the thresholds were set to 25 mV, providing a low threshold in boards implemented with BGM1013 amplifiers and a high threshold for a BGA2712 board.

Figure 7.16 shows the time differences between both sides of the BC11 and BC5 overlapped cells. Pictures represent the incident particles time profile along cells, showing a length of $\sim$2 ns as expected for these cells in the upper part of the box. Comparing both results the width of the cells are more clear with the STEP5.2 and even the noise out of the cell region disappears completely respect the STEP5.1, which profiles are clearly more noisy.

Figures 7.17 and 7.18 show the QtoW spectrums of both ends of both cells and the QtoW of one side of the cell vs the Qtow on the other side. Now the bump due to the streamers is clear. The different left and right shape, producing a non linear behaviour in the double plot, is due to the different preamplifiers used. The QtoW

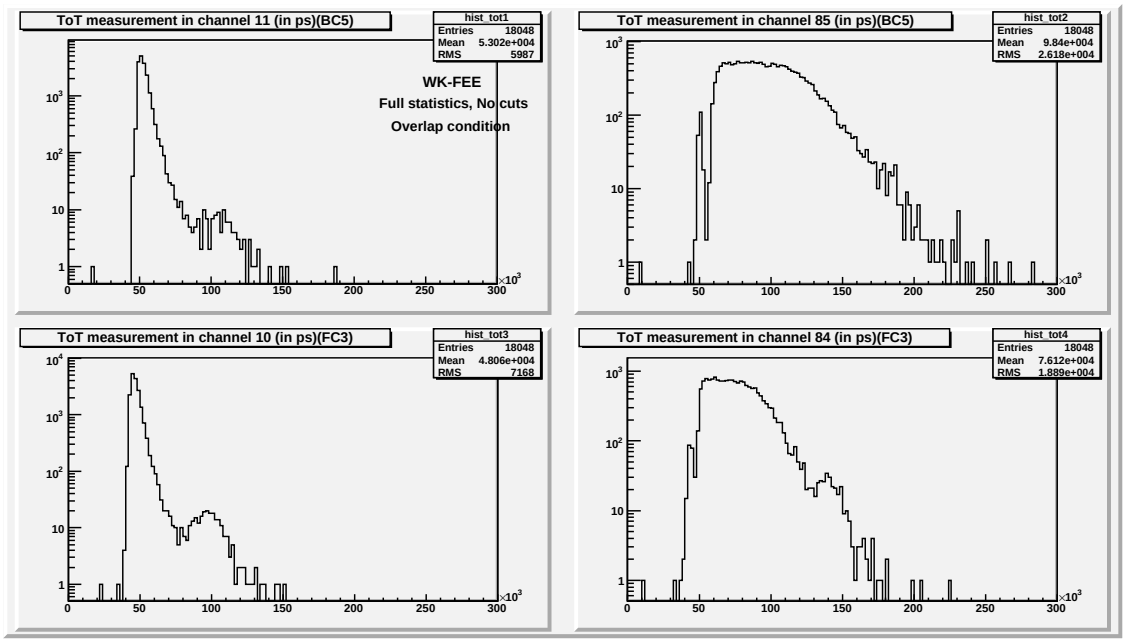


Figure 7.17: *QtoW spectrum for BC5 and FC3 overlapped cells using STEP5.2 boards. Left and right sides have different preamplifiers and different gains.*

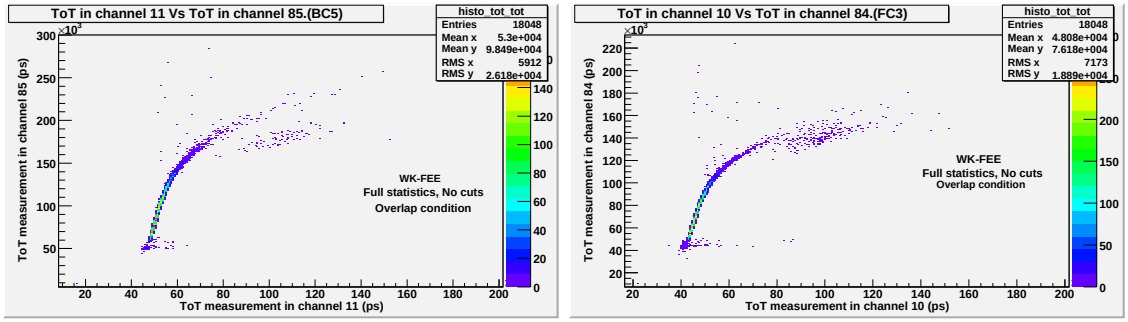


Figure 7.18: *QtoW measurements at both sides of BC5 and FC3 cells using STEP5.2 boards. Left and right sides have different preamplifiers and different gains, explaining the non-linear behaviour.*

spectrum of channels with a factor $G{\sim}10$ of gain is similar to the one measured in Nov05 test (see section 6.5), because the same amplifier was used in both cases.

Fig. 7.19 shows the time resolution before and after applying the slewing correction, together with the Δt as function of the QtoW after the correction. The last picture presents the behaviour of the time resolution along the time, showing no significant effects. The time resolution before and after the slewing correction are 80 and 78 ps/channel respectively, with $\sim$3% of 3σ tails. Although σ_T does not change significantly, tails are lower than with the STEP5.1 boards (we have more statistics in these detectors because the scintillator was centered over these cells).

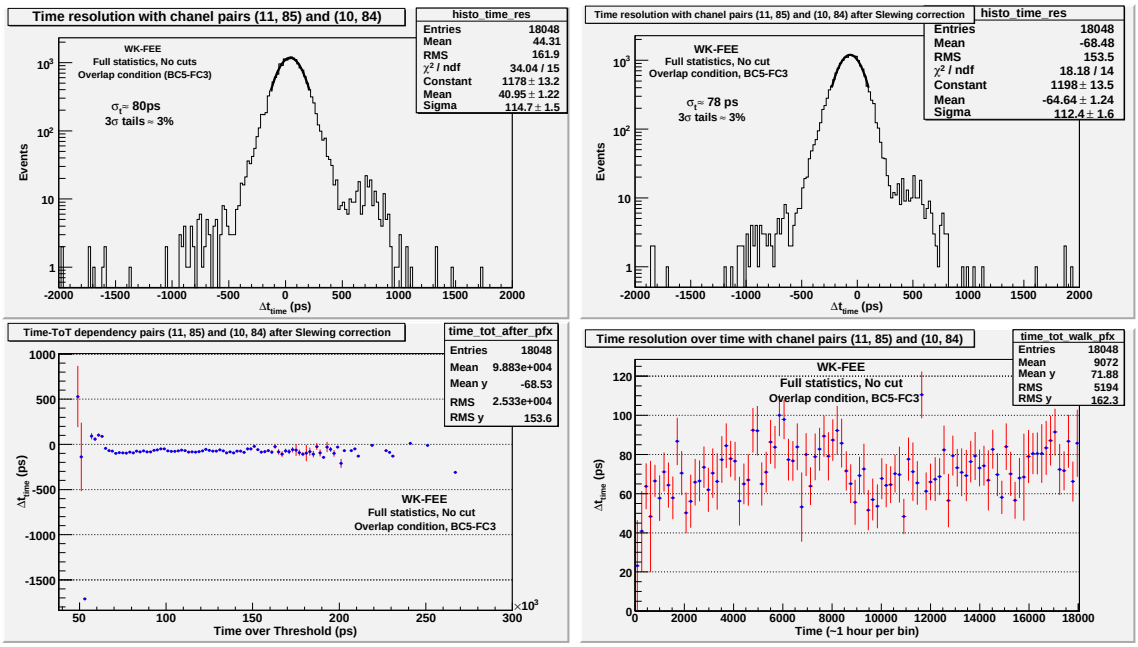


Figure 7.19: *Up: time resolution between BC5 and FC3 overlapped cells, before and after apply the slewing correction. Down: relation between time and the QtoW after the slewing correction (left) and the time resolution over the time (right).*

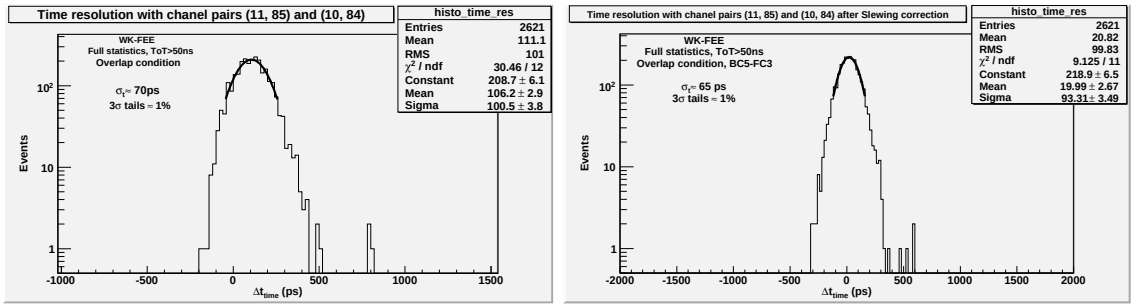


Figure 7.20: *Time resolution applying a cut for QtoW>50 ns on BC5 and FC3 overlapped cells using STEP5.2 boards.*

As was done for the BC11-FC9 pair cells, we may reject from the analysis some of the odd signals (either due to crosstalk effects or noise) doing a cut in QtoW>50 ns (approximate value of the QtoW output for zero charge signals). With this cut most of the crosstalk events and tails are rejected (as can be seen in Figures 7.20 and 7.21). Fig. 7.20 shows the time resolution before and after applying the slewing correction. The time resolution improves a little bit (65 ps/channel) and tails decrease even more (1% of 3σ tails). Fig. 7.21 shows QtoW spectrums at both ends of each cell.

Figure 7.22 shows the position resolution measured with and without the QtoW cut, providing both a similar $\sigma_{pos} \simeq 10$ mm, but reducing the 3σ tails from 3% to 1%.

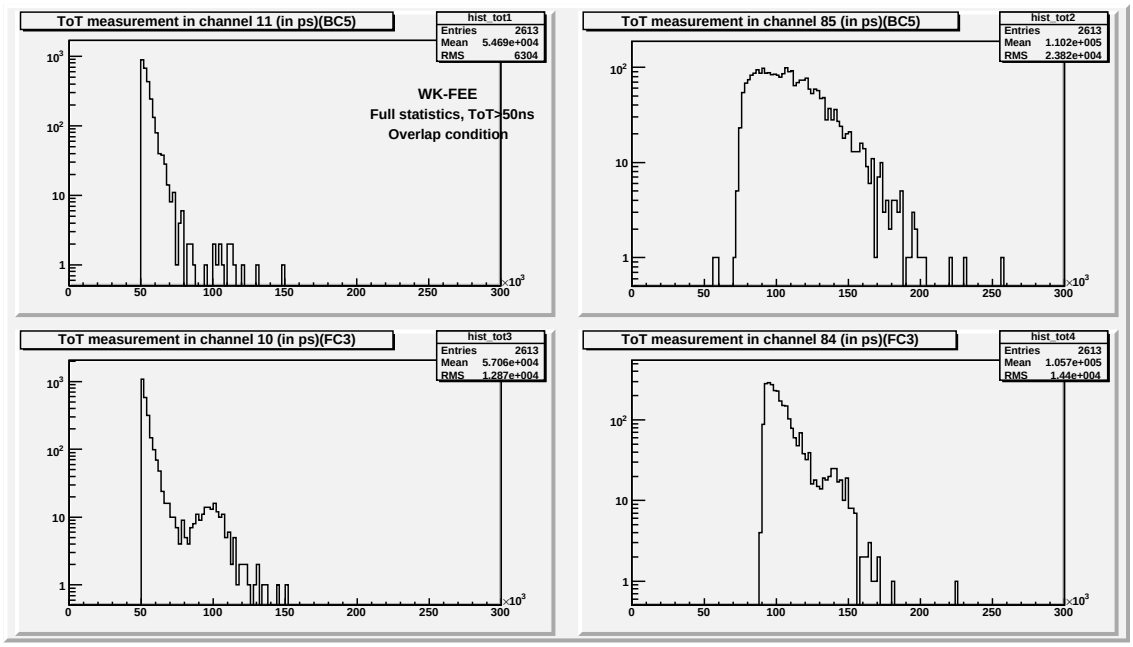


Figure 7.21: *QtoW spectrum with a QtoW>50 ns cut for BC5 and FC3 cells.*

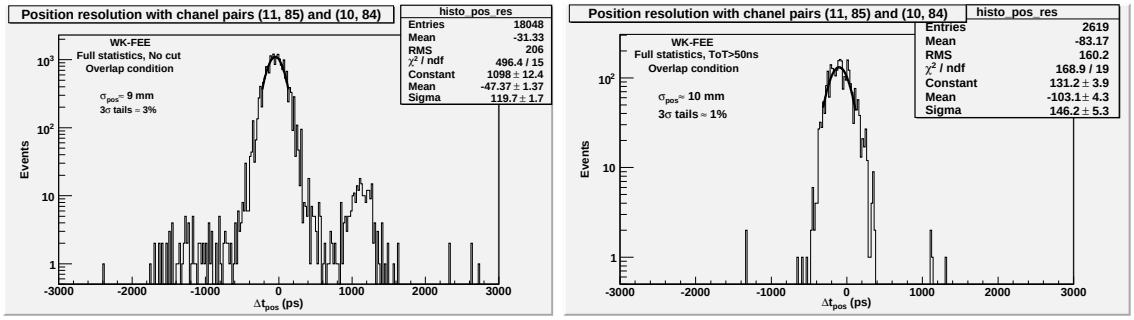


Figure 7.22: *Position resolution with full statistics (left) and with a QtoW>50 ns cut (right) using DBOs-STEP5.2, corresponding to the BC5-FC3 pair cells.*

Examples of RPC signals

Figure 7.23 shows some typical RPC signals measured at the output of the amplifier, including normal avalanches and several odd signals under various trigger conditions. Odd signals represents around 1% of the total. However, it dominates RPC coincidences due to the small cosmic rate on partially overlapping detectors.

Detector rate was dominated by the dark rate, i.e. self induced signals not triggered by charged particles. Most RPC detectors were not terminated with 50 Ω (open output), only the ones under investigation were connected to 50 Ω terminated electronics. This was a problem because it can produce reflections. However, the other output corresponding to the RPC under investigation was always connected to the FEE. Coincidence rate between left and right sides was close to 100%. In

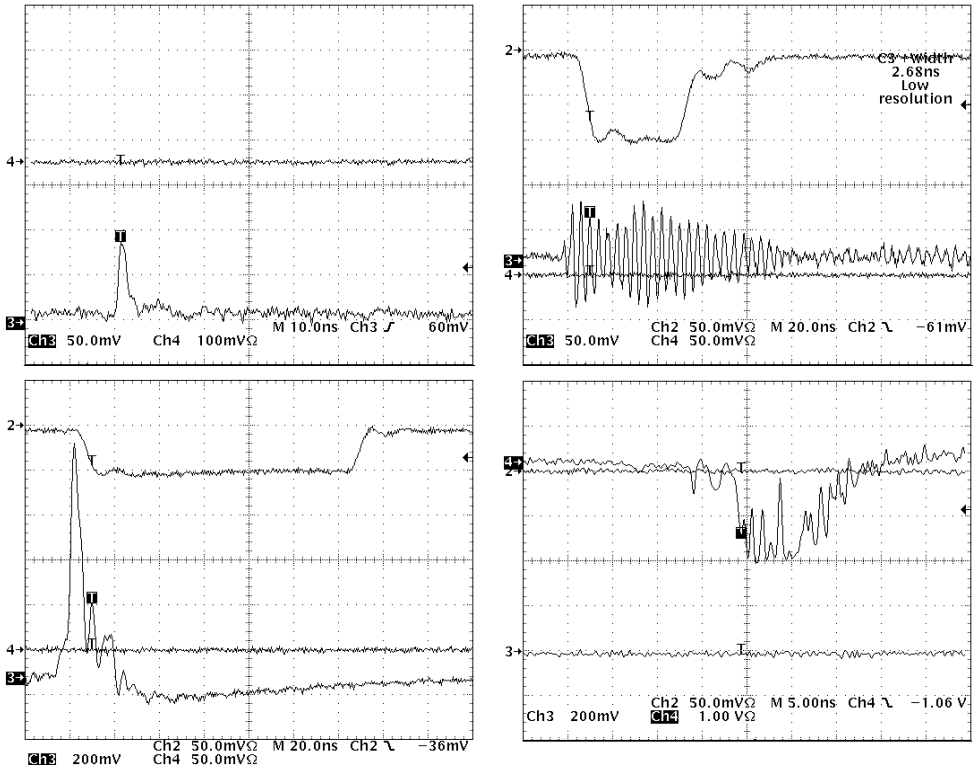


Figure 7.23: *Up: normal avalanche pulse at the output of the amplifier at channel 3 (left) and multiplicity 2 trigger signal at channel 2, corresponding to a crosstalk signal at channel 3 (right). Down: normal streamer signal at the output of the amplifier at channel 3, showing reflections inside the chamber (left) and an ugly streamer with precursor avalanches at channel 4 (right).*

the signals of Fig. 7.23 we did not observe any significant difference between both designs, although the discriminator of an unconnected STEP5.1 channel triggered sometimes on large streamers observed in a connected channel (not usual effect).

In the upper part of Fig. 7.23, the left picture shows a normal avalanche signal without any reflections. The right one shows an example of crosstalk. Crosstalk signals were the dominant source of multiplicity 2 events. Multiplicity 2 from cosmic rays measured by overlapping detectors is extremely rare, see section 6.5. Thus, observing coincidences between overlapping detectors due to cosmic rays requires an external trigger (plastic scintillator).

The upper Fig. 7.23-right shows two DBO fired channels (channel 2 shows the multiplicity output, 50 mV/fired channel). Channel 3 shows the amplifier output of one FEE channel, showing only a crosstalk signal at both sides of the cell. The width of the multiplicity trigger signals clearly shows that the integrated charge is close to zero, providing a ∼50 ns width corresponding to the minimum QtoW output for signals without charge (as expected for an oscillation). The width of the digital output for normal signals was around 50-70 ns. This is the reason we did the cut

in the analysis in QtoW>50 ns explained above, to avoid this crosstalk signals and oscillations. The *retriggering* without latching the signal is due to the method used for latching the discriminator output. It drives the LE and $\overline{LE}$ output away from each other after the latch is released. This prevents immediate re-latching.

The down part of Fig. 7.23 shows two different streamers signals. The left picture shows a big streamer (channel 3) reaching the saturation point of the amplifier (1 V). The channel 2 is the multiplicity trigger output (50 mV/fired channel): its width is about 120 ns. In this case, the trigger signal is multiplicity 1, showing that only one DBO channel is fired by this streamer. The right side shows a streamer observed for a very noisy RPC (high dark rate, extremely large fraction of streamers >10%). This signal was obtained with a different board, with the old two amplifiers DBO BGA2712 and GALI-S66 (with a gain $G\sim160$), giving inverted signals. Opposite end of RPC was terminated with 50 Ω and all other electronics were turned off. This streamer presents precursors before the real signal. Saturation of the amplifier is interrupted by reflections at 2 V (channel 4 is 1 V/dashed line).

Some signals shown above were obtained under bad operating conditions, making the dark rate and the amount of streamers unusually high. The observed signal quality changed on a daily basis depending on temperature and time. This behaviour is similar for both DBO designs, with different amplifiers and gains. Most likely the gas was not clean enough and special care on the gas quality should be taken.

7.4.4 Conclusions

In this test two slightly different DBO layouts of the same design were compared. The STEP5.2 was stable down to an effective threshold ETh[2] of 1.3 mV on a single channel, keeping noise-induced count rate low enough. Taking into account that this electronics has a signal amplification of $G\sim40$, the sensitivity exceeds the one used on previous beam tests ($G\sim50$ and threshold of 10 mV). The output pulse was clean. For the same conditions, the STEP5.1 was stable down to an ETh of 5 mV on a single channel. Tails were lower for the STEP5.2 board.

Regarding crosstalk, in the STEE5.1 board there was crosstalk (induced firing) between channels, mostly between channel 3 and the others. Based on previous experience, the reasonable ETh is estimated ∼25 mV. In the STEP5.2, no crosstalk was observed between left (1,2) and right (3,4) channels at an ETh=5 mV.

In view of its better stability, providing a safety margin for the scalability of the system, the STEP5.2 was chosen for the final design. On what concerns the QtoW behaviour, studies were made as a function of the charge. It was found a good response for small charges, failing to clearly separate the streamers from the normal avalanches (as was shown in previous tests), clearly separated in charge. This is the main feature that required some improvements.

[2]Effective Threshold is the real threshold after subtracting offsets.

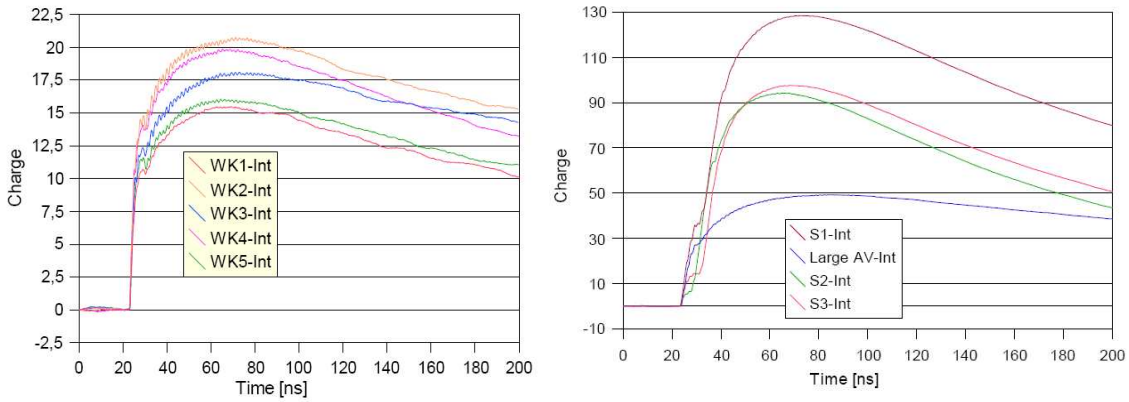


Figure 7.24: *Simulation of the charge at the output of the amplifier for large normal avalanches (left) and huge avalanches and streamers (right).*

7.5 QtoW improvements of the DBO-STEP5

In order to improve the RPC-FEE behaviour in the streamers region and easily separate them from the normal avalanches, a simulation based on already measured signals in the previous test and an investigation with real DBOs using different values of the differentiating elements were developed. The same conclusions were obtained for both studies.

7.5.1 Simulation based in real signals

The simulation done is complementary to the one presented in chapter 5 for negative signals, applying changes in the original design and it is based on real signals. The digitized amplifier signals can be transformed mathematically and put into a simulation of the integrator. This simplifies the analysis of systematic changes of electronic components. As was shown in section 7.4, the reduction of the width for streamers as compared to large avalanches was still clearly visible. A negative undershoot of the amplifier output (more pronounced for streamers) remained. This is clearly visible in the (numerically) integrated amplifier output (Fig. 7.24).

Figure 7.24 shows the simulation of the original settings via mathematical reduction of the differentiation of the measured signals for large normal avalanches (left) and huge avalanches and streamers (right). The blue line has a different tail behaviour. Maybe it is a self induced avalanche with a different ionic tail behaviour. Even ideal (mathematical) integration of streamers and a huge avalanche results in a nearly indistinguishable charge after 200 ns integration time for the DBO-STEP5.2 version (blue, green and red curves). This is due to the differentiation of the saturated amplifier output (in case of streamers). After 220 ns streamer charge (green, red) will be below the charge of the large avalanche (blue).

As conclusion, some improvements are required to optimize the FEE features:

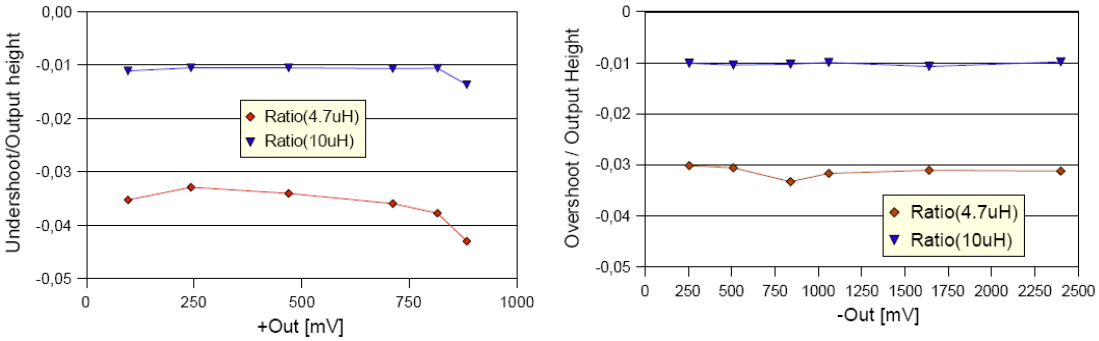


Figure 7.25: *QtoW analysis. Left: undershoot of the amplifier output for positive signals. Right: overshoot for negative signals, both for two different inductances.*

- Reducing the undershot to basically zero, increasing the inductance attached to the amplifier. This does not help to get streamers out of the width tail generated by large avalanches but the reduced undershoot results in a larger width. This gives more weight to the undershoot with its large time constant.

- Increasing the value of the integrating capacitor to 1.5 pF instead of 1 pF. This results in a larger decay time (longer memory on the positive part of the signal), decreasing the maximum height of the integrator output. Thus, the width of the signal is not increased.
  Since the reduction of the undershoot at short times (20% increase of the integrated signal at 80 ns) increases the sensitivity to small avalanches, the smaller gain of the integrator is compensated for small signals. This keeps the sensitivity of the width for small signals although the gain of the integrator is reduced. The latter avoids saturation of the integrator for large signals. The coupling capacitors between latch enable and discriminator output were also tuned: $\overline{LE}$ to $\overline{Q}$ from 27 to 30 pF, providing a longer decay time of the 2nd integration and LE to Q from 47 to 39 pF, giving a slightly smaller base width.

- Avoid saturation of the amplifier output for large signals and streamers. This requires to go to negative pulses (amplifier saturates at ∼0.85 V for positive signals but provides up to -2.5 V output signals for negative polarity).

- Reduce hysteresis of the discriminator to a minimum: 39 kΩ instead of 33 kΩ. This allows for lower effective thresholds.

Results obtained reducing the undershoot increasing the inductance attached to the amplifier are shown in Fig. 7.25. The left picture shows the ratio between the signal and the undershoot for a fast input signal without reflections and without ionic tail for positive signals. The red and blue curves present, respectively, the results for the 4.7 and 10 μH inductor values used as a pull up element for the amplifier. The right plot shows the same values for negative signals and the overshoot. Replacing

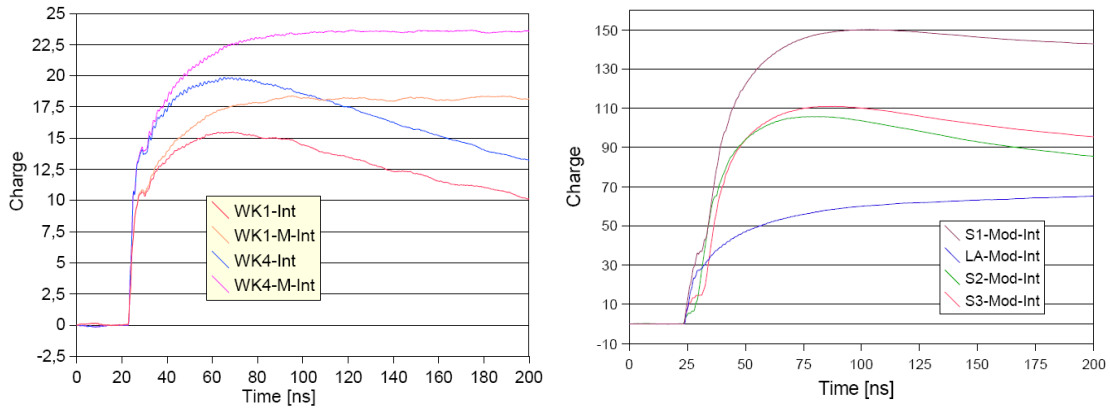


Figure 7.26: *Left: integrated signal of small and medium charges avalanches without modifications besides a correction of the baseline shift (red, blue) and mathematically reduced differentiation of the the same measured signals (orange, magenta). Right: the same analysis applied to streamers and huge avalanches.*

the 4.7 μH inductor by a 10 μH inductor decreases the negative undershoot of a short signal (pulser with 2 ns of rise/decay time) by about a factor 3. A more realistic pulser setting including reflections and an ionic tail shows that the signal undershoot for the 10 μH version is slightly overcompensated by the ionic tail.

Figure 7.26 shows the results of a simulation done with a larger inductor, reducing mathematically the differentiation of the measured signals. The left picture shows the integrated signal of normal, relatively large avalanches without modifications, besides the same measured signals corrected through the baseline shift (red and blue signals) and the mathematically reduced by differentiation (orange and magenta ones). The reduction was chosen to minimize overshoots or undershoots. The same procedure was applied to streamers (S1-S3) and a huge avalanche (the right picture). The reduced differentiation results in a larger gap between the integrated signals after 200 ns as compared to the original signals (see Fig. 7.24). However the different slopes remain and force the integrated streamer charge to decay faster than normal avalanches. Thus, for large signal width's above 200 ns the streamer charge can still fall below a significantly smaller avalanche (taking the maximum of the integrated charge as a measure of the avalanche size).

Results corresponding to the first and the second point (providing a wider digital output signal) are shown in Fig. 7.27. It shows an increase of the discriminator output width as function of avalanche charge. Charge was estimated by using the maximum of the integrated signals obtained with the same amplifier. Different charges were obtained by scaling the same (measured) avalanche. Simulation bypassing the amplifier stage. Integrator feedback capacitor was set to 1.5 pF instead of 1 pF. $\overline{Q}$ to $\overline{LE}$ capacitor was increased from 27 to 30 pF (2nd integration) and Q to LE capacitor decreased from 47 to 39 pF (steeper crossover). The capacitor

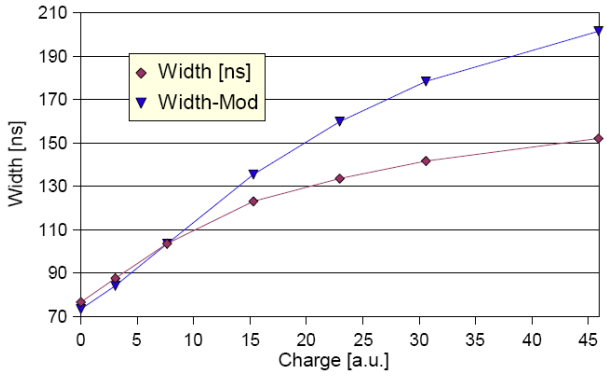


Figure 7.27: *Width-to-charge for the settings investigated in the test of February at GSI (red) and after the modifications at the LE and the integrator (blue).*

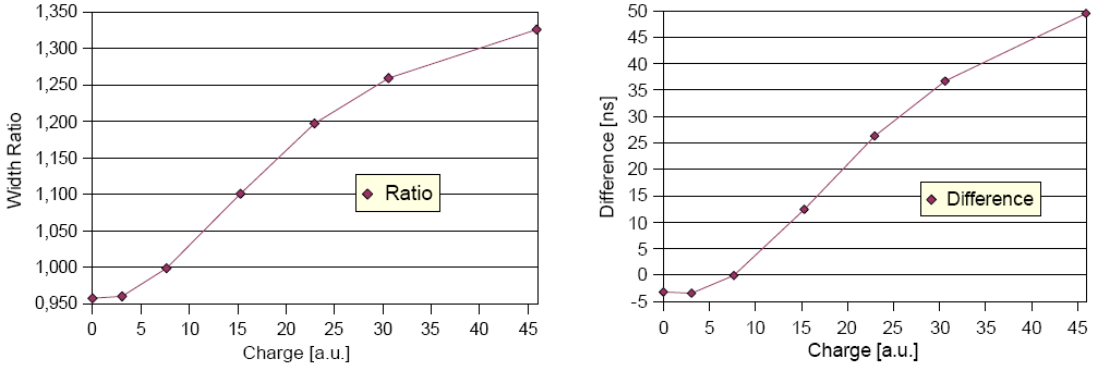


Figure 7.28: *Left: ratio of modified output width respect to original width (after modifications). Right: increase of the output width in ns after the modifications.*

connecting the $\overline{LE}$ to the $\overline{Q}$ of the discriminator acts as a second RC integration stage of the integrator output. The change of inductor was estimated by decreasing the differentiation of the measured amplifier output mathematically. Fig. 7.27 shows the width to charge of the original configuration (red) and the modifications (blue).

Fig. 7.28-left shows the ratio of modified output width respect to original width (after applying modifications). The ratio contains slightly different offsets of ∼75 ns for charge zero. The right plot shows the increase of the output width in ns after the modifications. The scaled amplifier output reaches values beyond the amplifier saturation for the largest charge. Saturation effects are not included in the scaling procedure. Furthermore the minimum width of ∼75 ns fits nicely to the location of the maximum of the integrated charge. This results in a high sensitivity of the output width to small charges.

These modifications were applied to large avalanches and streamers. Results with real signals are shown in Fig. 7.29. Reduced differentiation was obtained mathematically (real inductor will have frequency dependent inductance). This might result in further improvement. Fig. 7.29-left shows the width as function of the charge.

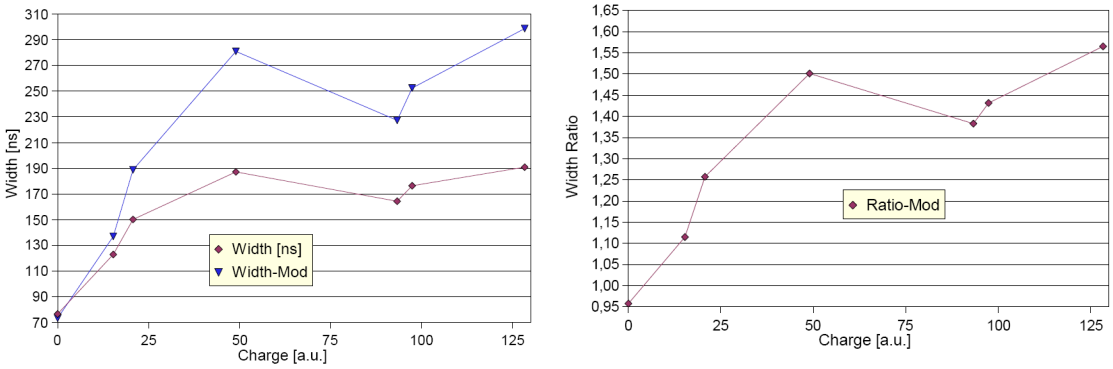


Figure 7.29: *Left: width-to-charge for the original settings (red) and after the proposed modifications (blue). Right: ratio of modified output width to original width, both for large avalanches and streamers.*

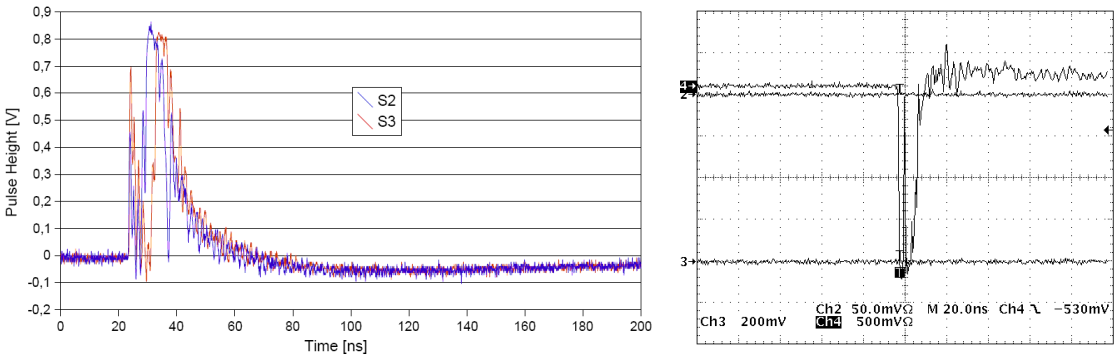


Figure 7.30: *Amplitude for two positive streamers signals (left) and a negative streamer signal (right), showing the lower saturation point for positive ones.*

The points above Q=80 a.u. are unambiguously streamers with precursors. They all drive the amplifier into saturation for a long time. The point at Q=50 a.u. is an unusual large avalanche with a long tail. The right picture presents the width-ratio as function of the charge, showing that streamers are better separated from large avalanches with the modified version. Also the 2nd point seems to be large avalanche. Charge is in arbitrary units calculated from the maximum value of the mathematical integral obtained by the amplifier.

We also did some analysis related with the amplifier polarity. The saturation of the amplifier (practically all streamers) reduces the separation of streamers from large avalanches since the signal undershoot gets larger for saturated signals (Fig. 7.30) and the positive part is reduced. Thus, working with negative signals -having a factor 2.5 larger dynamic range of the amplifier- is an advantage. For negative signals the amplifier output reaches 2.5 V while for positive signals it saturates completely at about 0.9 V (depending on pull-up inductor/resistor, Fig. 7.30).

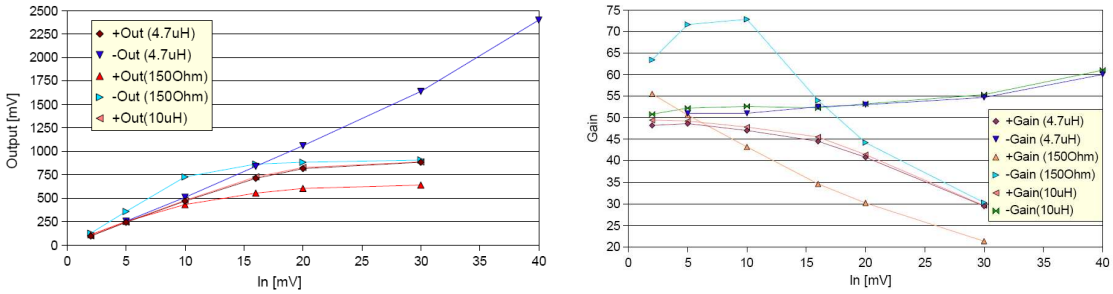


Figure 7.31: *Amplifier output (left) and amplifier gain (right) as function of the input for different pull-up elements.*

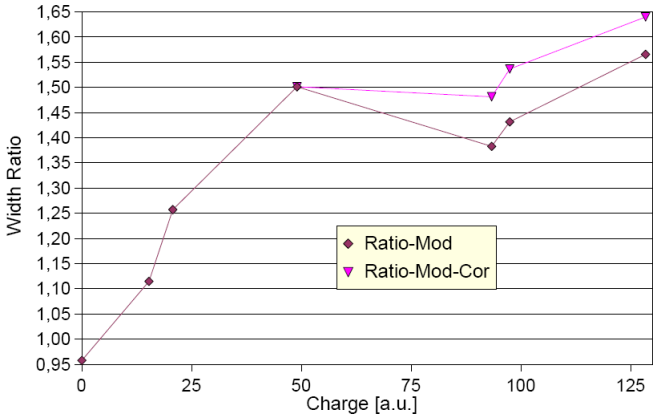


Figure 7.32: *Width ratio comparison as function of the charge for previous modified settings and negative streamer signals.*

Figure 7.31-left shows the amplifier output as function of the input voltage. +Out/-Out refer to positive and negative input signals, respectively. Measurements were done for different pull-up elements of the amplifier (both inductors and resistors). The right picture shows the same results normalizing the output to the input signal (gain of the amplifier). As is shown, the gain is constant around a factor $G{\sim}50$ with negative polarity signals (before the saturation at -2.5 V) and inductors as pull-up of the amplifier.

Unfortunately, the measurement of large avalanches and streamers with the oscilloscope was hampered by the oscilloscope vertical range. The latter resulted in saturation of the measurement for negative pulses due to the limited oscilloscope vertical range (0.79 V). However, the measured gain ratio for positive and negative signals allows to correct the measured positive streamer pulses assuming a negative pulse. Results are shown in Fig. 7.32. The magenta line shows the improvement for streamers after saturation effects were taken out of the measured data (conservative approach for the correction of the saturation effect). This result corresponds roughly to measuring negative signals (reversed HV polarity of the RPC).

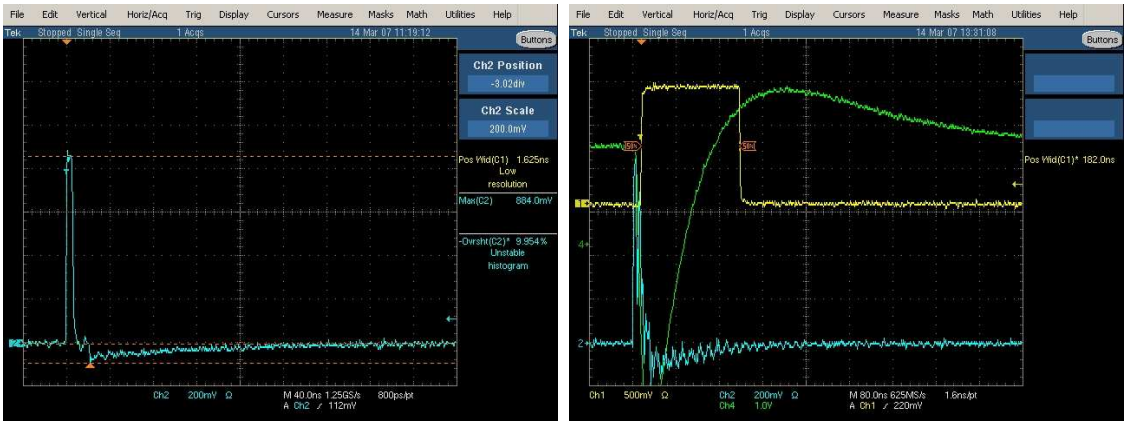


Figure 7.33: *Original DBO-STEP5 channel. Left: saturated output signal of the amplifier for test signals, showing its undershoot. Right: analog (blue), integrated (green) and digital (yellow) signals for a streamer RPC signal.*

As summary, the sum of all these modifications as compared to the original version seems to increase both the sensitivity to small signals and for streamers, simultaneously. Although some tests with real signals and the FEE were still required.

7.5.2 FEE analysis with test and RPC signals

Tests with the 3-cell RPC prototype [64] were developed using the following experimental setup: in one side of a RPC cell we connected a BGM1013 preamplifier and on the other side a DBO channel. Both signals were sent to an oscilloscope and analyzed. The integration of the preamplifier signal provides the charge of the RPC signal and the DBO provides the digitized width. The HV applied to the RPC was changed between 5800 and 6000 V to analyze the streamers. The same setup was implemented with test signals, although we only analyzed the amplifier, the integrator and the discriminator signals behaviour. We tested different configurations, but all of them for 10 nF and 100 nF coupling capacitors of the preamplifier.

Channel with original settings

First of all, a channel with original settings (the same used in the previous test) was tested. This means a 10 nF blocking capacitors of the BGM1013 amplifier and an inductance L=4.7 μH acting as pull-up. The output of the amplifier saturates at the maximum value working for positive signals (∼900 mV). In this configuration, the undershoot at the output of the amplifier is more important. Fig. 7.33-left shows an example with test signals, saturating the amplifier. For all these measurements, we used the asymmetric RC-time constants of the simulation for the LE and $\overline{LE}$: R=1.5 kΩ for $\overline{LE}$ and R=1.8 kΩ for LE, both with C=47 pF. This results in a larger base width of the discriminator, improving the width response to small signals.

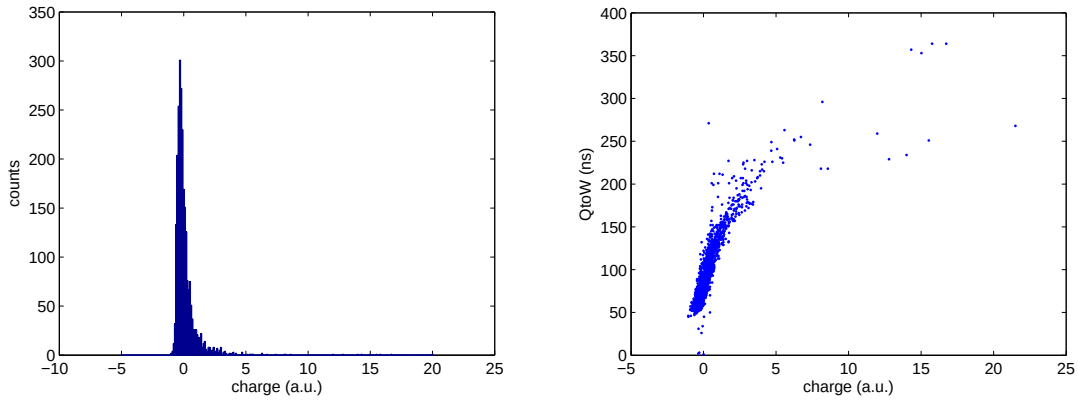


Figure 7.34: *Original settings of one STEP5 channel with RPC signals. Left: charge spectrum, after subtracting the pedestal. Right: QtoW as function of the previous charge. Charge is in a.u.*

With real RPC signals we measured the QtoW behaviour acquiring with a digital Tektronix oscilloscope. The charge and the width were calculated with MATLAB. The ToF threshold was set to -20 mV in all measurements. Fig. 7.33-right shows the outputs of the amplifier (blue), the integrator (green) and the digital signal (yellow). It is clear the overshoot for these settings, more pronounced for bigger signals. Due to the fact that the integrators have also built in decay constants, the undershoot can overcompensate the larger positive signal (which appears earlier and its effect on the integrator decays with the time), producing digital signals with a smaller width for streamers than for big avalanches even with smaller charges.

Figure 7.34 shows some results regarding charge spectrum (left picture) and QtoW (right side) as function of the charge. The charge is calculated extracting the pedestal of the analog signals by software. This right plot shows the odd behaviour for streamers signals (also seen in previous test), clearly separating the different regions for normal avalanches and streamers. Streamers with larger charge than a large avalanche show smaller width, due to the large undershoot produced by the differentiating pull-up coil of the amplifier. Points with QtoW>300 ns are large avalanches driving the amplifier (positive signal) into saturation. Points with charge Q>8 a.u. and width between 200 and 300 ns show streamers (identified via precursors of different intensity). All streamers drive the amplifier into saturation. This is the behaviour we want to analyze to avoid it in our electronics.

As was already shown in section 7.4, the current amplifier/integrator combination does not allow to clearly identify streamers (see the behaviour in Fig. 7.18). At lower gains (left figures), streamers are clearly separated from normal avalanches, whereas for the higher gain (right figures) the width for streamers is pushed into the tail of the normal avalanche distribution. A lower amplifier gain is definitely not the solution, but it indicates in which direction to go in order to make the improvement.

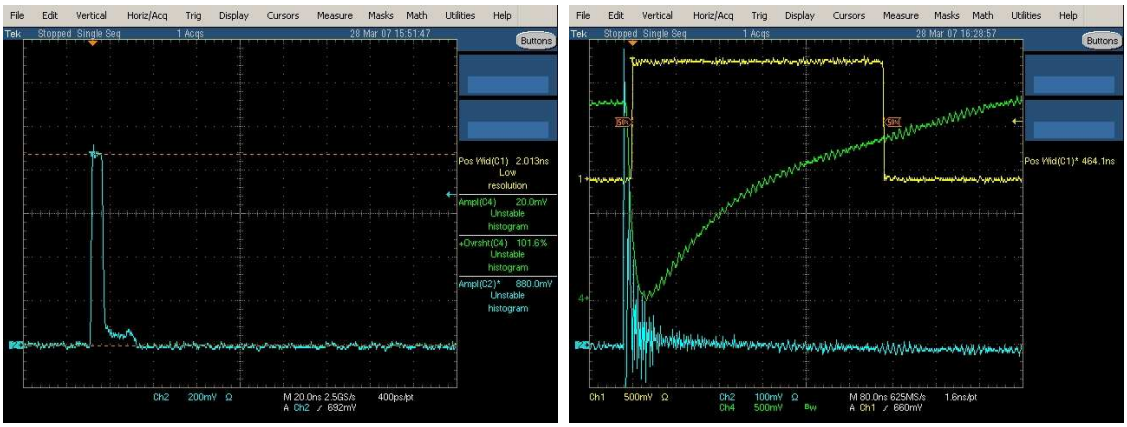


Figure 7.35: *DBO-STEP5 channel with C=100 nF and L=22 μH. Left: saturated output signal of the amplifier for test signals. Right: analog (blue), integrated (green) and digital (yellow) signals for a big avalanche.*

Channels with modified settings

In order to avoid these problems, several tests were done. The first one was to increase the blocking capacitors of the BGM1013 amplifier. With this change we tried to reduce the undershoot at the output of the BGM1013, generating larger width signals for streamers. Other change tested was taking a larger inductor as amplifier pull-up, making sure that *re-triggering* on ionic tails of normal avalanches does not occur (making inductor not too large). With these capacitors, different configurations were also tested for the RF-choke at the output of the amplifier: different inductance values (from L=4.7 μH until 40 μH) and also replacing the inductance for a 150 Ω resistor (as was done in simulation). The value of the inductor can be used to fine-tuning the output impedance.

In order to improve the QtoW behaviour, the best choice was to increase the original 4.7 μH inductance of the amplifier, although taking care of not increasing the range width of the QtoW to avoid increasing the jitter in the trailing edge of the digital output signal. The test shows that the jitter is higher for bigger inductances, making worse the accuracy of the QtoW measurements because the cross point of LE and $\overline{LE}$ signals is more flat making also bigger the uncertainty in the measurement.

The final configuration chosen was a 100 nF blocking capacitor together with a 22 μH RF-choke, being the jitter in the trailing edge still ∼200 ps, acceptable for our purposes. Regarding the amplifier output, it also saturates at the maximum value (∼900 mV). With this inductance, undershoot is clearly lower than the one obtained with the original settings (see Fig. 7.35-left, showing the amplifier output for saturated test signals). Fig. 7.35-right shows the output of the integrator (green), the amplifier (blue) and the digital signal (yellow). The overshoot of the integrated signal is even better than with other settings, being the digital output wider.

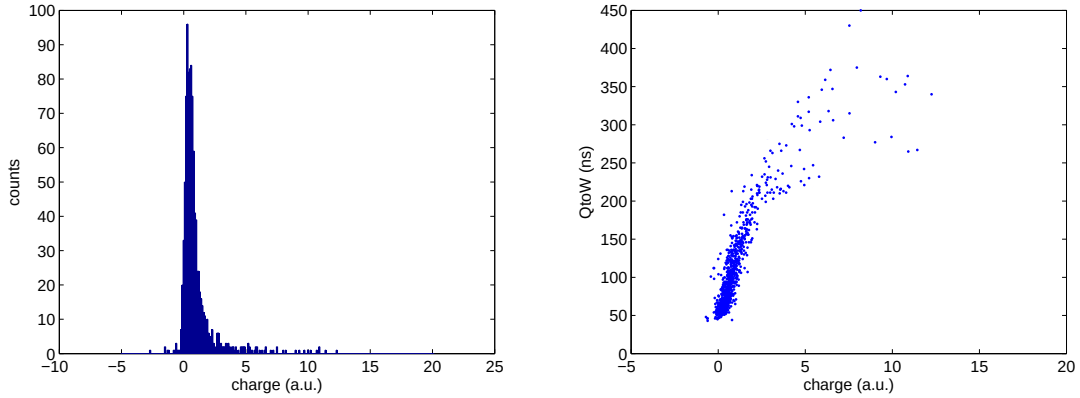


Figure 7.36: *DBO-STEP5 channel with C=100 nF and L=22 μH. Left: charge spectrum, after subtracting the pedestal. Right: QtoW as function of the charge.*

Figure 7.36 shows some results regarding charge spectrum and QtoW as function of the charge. Increasing the inductance to22 μH, the digital output is wider (the QtoW range changes between 40 and 450 ns, ∼80 ns bigger than with original settings). For streamers signals the behaviour seems to improve respect using lower inductances, showing a less pronounced behaviour for streamers (although the dispersion is increased). Unfortunately, it remains the effect that the width of streamers is smaller than for avalanches with comparable charges because a negative undershoot of the amplifier output (more pronounced for streamers) still remained.

This new design was tested in beam and with a ^{22}Na source at GSI in June 2007.

7.5.3 QtoW improvements in-beam environment

Data presented on this section were taken in a beam time done at GSI in June 2007 and with a ^{22}Na source in order to analyze the QtoW behaviour in real conditions, mostly with streamers and big avalanches. The specific conditions of the setup were:

- We used two cells (one in each layer) of the RPC sector used in Nov05 beam time. The HV applied on the cells was 6000 V, although some tests were done increasing the HV until 6400 V.

- The setup was implemented with two different electronics: a reference electronic from LIP with only one preamplifier with a R=150 Ω as pull-up for charge measurements and a DBO for QtoW measurements with an inductance of 22 μH as pull-up. Both electronics were connected at each side of one cell. The ToF threshold was set to -10 mV and the LE baseline to ∼250 mV.

- Four signals were recorded on a digital oscilloscope: both digital signals (from 2 DBO channels) and both analog signals (from 2 reference channels). Data were taken triggering by an external coincidence unit doing coincidences be-

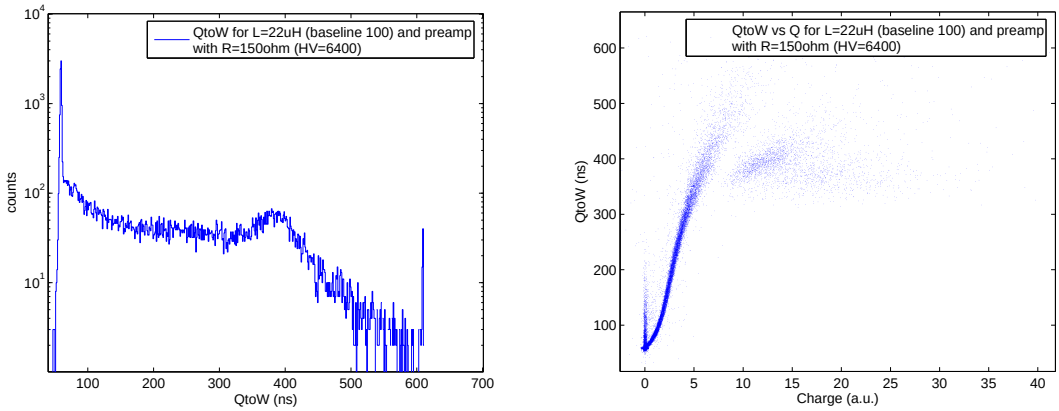


Figure 7.37: *Left: QtoW spectrum. Right: QtoW (ns) vs charge (a.u.), both with a L=22 μH as pull-up of the amplifier and the reference electronic with a R=150 Ω as pull-up. HV was set to 6.4 kV.*

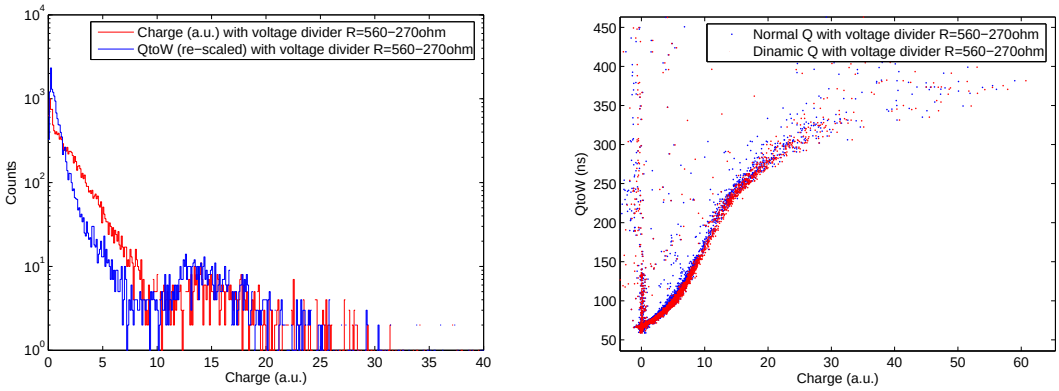


Figure 7.38: *Left: QtoW and charge spectrums. Right: QtoW (ns) vs charge and dynamic charge (a.u.), with a voltage divider of 270-560 Ω before the integrator. The reference electronic with a R=150 Ω as pull-up. HV was set to 6.0 kV.*

tween the signals coming from an external scintillator (placed on the back of the box) and the digital signals, which were split with a star terminator.

Data were taken with beam and with ^{22}Na source, using data took with beam in order to compare if the QtoW behaviour is comparable in both cases. The HV of the cells was set to 6.4 kV to differentiate between normal avalanches and streamers. The DBO channel has an inductance L=22 μH as pull-up of the amplifier and the LE baseline was set to ∼250 mV. The ToF threshold was set to -10 mV for these measurements. Fig. 7.37 shows the QtoW spectrum (left) and the QtoW behaviour as function of the charge (right) in beam environment. QtoW behaviour as function of the charge is similar to the one obtained with ^{22}Na source (see Figs. 7.34 and 7.36). Both pictures show clearly the streamers at QtoW∼400 ns. Taking this plots as reference, we continued the QtoW improvements with a ^{22}Na source.

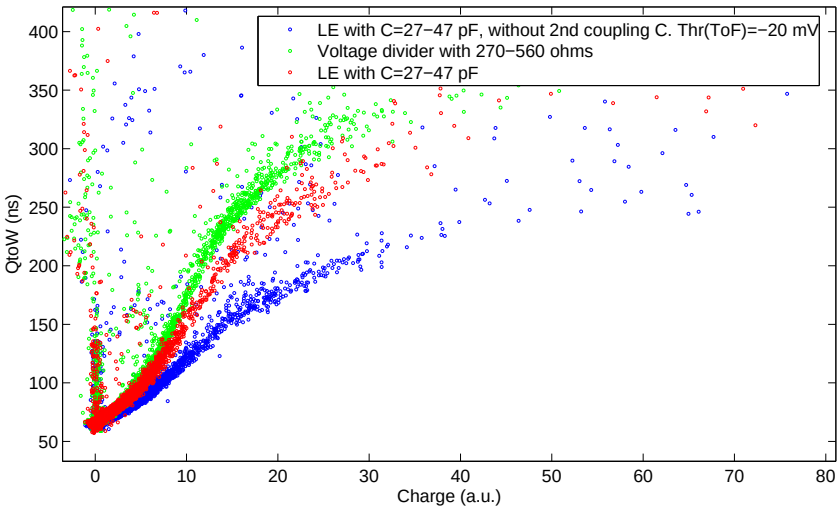


Figure 7.39: *QtoW (ns) vs charge (a.u.) for different cases: a) with a voltage divider of 270-560 Ω before the integrator (green), b) with a LE capacitors of 27-47 pF (red) and c) the same without the second coupling capacitor and Thr(ToF)=-20 mV (blue). HV was set to 6.0 kV.*

The first test done was to increase the RC of the integrator, decreasing the maximum height of the integrator output putting a C=3.3 pF and a R=12 KΩ. Furthermore, it was also needed to decrease the width range of the QtoW (Fig. 7.37-right) to try to get a common QtoW behaviour for normal, high avalanches and streamers. For this purpose, we implemented a voltage divider before the OPA690 integrator and after the output coupling capacitor of the BGM1013 amplifier, adding one 270 Ω resistor to ground at the original resistor R=560 Ω.

Figure 7.38 shows the results corresponding to those values. The left picture presents the projection of both QtoW and charge spectrums in the same plot, having a similar behaviour. The right picture shows the QtoW as function of the charge calculated in two different ways: i) a normal way with a fixed window at the scope and ii) a dynamic way, changing the window for the analog signal. The right plot shows that there are not significative differences between both ways. The plot show, clearly, a decreasing in the QtoW range, varying between 50 and 450 ns compared to 50 and 600 ns in the original settings (Fig. 7.37). The saturation effect is also clear, due to the saturation of the amplifier. Finally, the QtoW behaviour as function of the charge improved, showing only one behaviour at the whole QtoW range, including the streamers for Q>15 a.u. and QtoW>250 ns. The HV was set to 6.0 kV.

More tests were done trying to improve more the QtoW behaviour taking previous setup as reference. The different configurations used were the following:

- The same presented in Fig. 7.39, with the voltage divider 270-560 Ω (green curve) before the OPA690 op-amp working as integrator.

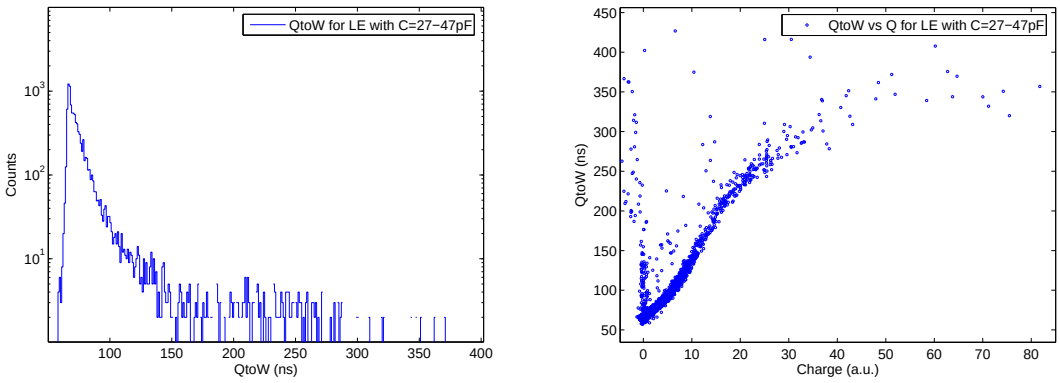


Figure 7.40: *Left: QtoW spectrum. Right: QtoW vs charge (a.u.), both for LE and $\overline{LE}$ to C=47 pF and 27 pF, respectively, and the reference electronic with a R=150 Ω as pull-up. HV was set to 6.0 kV.*

- The previous configuration connecting the outputs of the discriminator and LE and $\overline{LE}$ to C=47 pF and 27 pF, respectively (red curve).
- Removing the second coupling capacitor (2.2 nF) at the amplifier output for this last configuration (blue curve) in order to check if it is required.

Results showing the dependence of the QtoW with the charge for a ^{22}Na source for all these configurations are presented in Fig. 7.39. In the last run the ToF threshold was increased from -10 to -20 mV to avoid *retriggers* in the discriminator, showing the necessity of this second coupling capacitor before the MAX9601 discriminator. In the other two runs, the QtoW behaviour is similar, showing an improvement in the streamers region. The main differences between them are the smaller QtoW range and also the small dispersion in the streamers for the configuration with LE capacitors of 27-47 pF. As this configuration seems to be more robust, it was chosen for the final version.

Figure 7.40 shows the QtoW spectrum and the QtoW as function of the charge for the final configuration. The QtoW spectrum shows that the minimum QtoW is lower than in previous runs. Streamers seem to be clearly separated from normal avalanches (QtoW>200 ns) and the QtoW behaviour as function of the charge improves, showing only one QtoW region and smaller dispersion in the streamers.

The time resolution between two cells was corrected using both analog charge and QtoW information. Results are shown in Fig. 7.41. The time resolution achieved is basically the same independent of the correction applied, showing 82 and 80 ps/channel after charge and QtoW corrections, respectively. The only difference between both corrections is the number of tails which worsened applying QtoW corrections from 5% (with charge) to 10% 3-σ tails. Time resolution and position calculated with this method are free of structures.

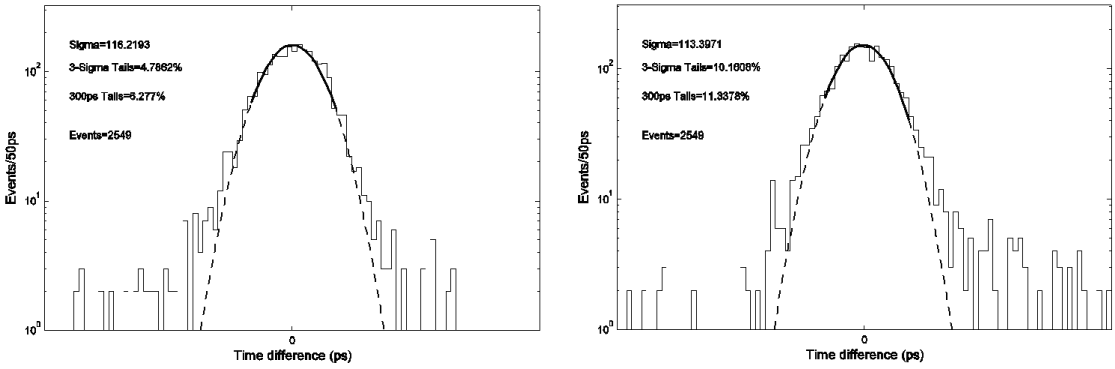


Figure 7.41: *Time resolution combined corrected with analog charge (left) and applying QtoW algorithm (right).*

7.6 First RPC sector installed in HADES

The performances of the tRPC system were analyzed with a fully instrumented sector installed in its final position at the HADES spectrometer [107], [56], exposed to particles coming from reactions of a ^{12}C beam on Be and Nb targets at 2 GeV/A kinetic energy. The FEE was also characterized using narrow test signal pulses.

The block diagram of the setup used in this test is shown in Fig. 7.42-left, where two different parts can be distinguished: the RPC+FEE and the DAQ systems.

7.6.1 FEE boards

New DBO and MBO boards were developed, including only a few modifications respect previous designs. One full RPC sector requires 108 DBOs and 16 MBOs.

The new DBO included the improvements shown in section 7.5. It is only a small modification of the previous DBO-STEP5 design [56]. In the analog step only two changes were done: to increase both the input/output coupling capacitors of the BGM1013 amplifier from 10 to 100 nF and the inductance used as pull-up of the amplifier from 4.7 μH to 22 μH. The 2.2 nF capacitor before the MAX9601 discriminator input was kept to reduce the noise injection at the input of the discriminator. In the integration step the RC constant was changed slightly, setting R=12 kΩ and C=3.3 pF. In the digital step we changed the capacitors of the latch enable inputs of the discriminator, connecting LE to C=47 pF and $\overline{LE}$ to C=27 pF.

The new MBOv3 [56], [57] has only some modifications respect previous version. Basically, we added a thick cooper ground trace on the bottom layer to improve the grounding with the detector aluminum box (via beryllium gaskets, see Fig. 8.4), some filters in common mode for filtering noise and the op-amp inverters to get negative ToF thresholds required in the new design. Groups of four MBOs are connected to the same time-to-digital converter readout board (TRB) [86], which is part of the HADES acquisition system.

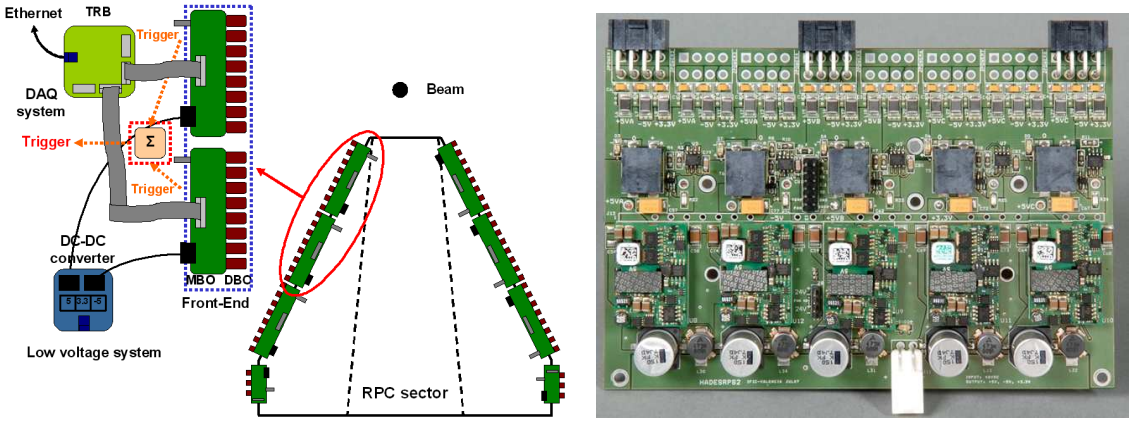


Figure 7.42: *Block diagram of the whole system in the first integration of one RPC sector in the HADES spectrometer (left), together with the first version of the Low Voltage board (right) which feeds the FEE boards (size 20×15 cm^2).*

FEE boards are powered by a new low voltage board [108], developed by A Gil at IFIC, based on switching DC-DC converter modules, which are prepared for voltage and current monitoring (Fig. 7.42-right), being powered by 48 V at the input.

These boards were tested for the first time in this beam time. Two boards are enough to feed a full RPC sector. The power sub-systems can be distributed along the detector and located close the load, which will reduce significantly both the length of the cables after the LV boards and the power losses associated to the voltage drops caused by cable transmission. The short cables help to reducing the noise picked up by them and conducted to the load.

The system is designed with a distributed architecture and contains custom Low Voltage boards based on Tyco DC-DC switching converters to obtain a higher efficiency and a much compact design as compared with laboratory linear supplies. The switching converters are conveniently filtered to reduce EMI, providing an output ripple/noise of 0.1% of the nominal output voltage at 20 MHz bandwidth and noise levels of the order of 1 mV RMS at 1 GHz. In order to minimize noise, we added some ferrites with low ESR multi-layer filter capacitors [104]. In this way, the high impedance of the ferrites at high frequencies is combined with the low impedance of the capacitors to create a resistor divider with a very high reduction factor at high frequencies. A common mode choke and a ferrite bead together with multi-layer capacitors were used for further noise reduction at high frequencies.

The control system and monitoring was integrated in the slow control of the experiment, being the monitoring of the 48 V power supplies done via LXI-LAN interface. Each LV board provides voltage and current monitoring at the output of each DC-DC converter, together with temperature monitoring in order to fast detect critical failures. The interface used is a 1-wire bus, allowing the monitoring of all the LV boards with a custom general purpose control board based on a microcontroller.

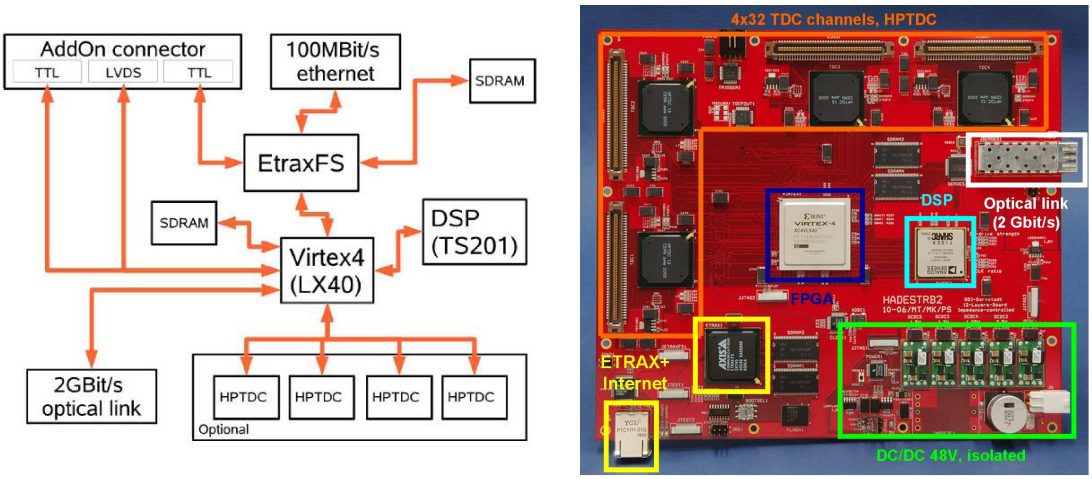


Figure 7.43: *TRBv2 block diagram (left) showing its main features and module picture (size 20×23 cm^2) for the DAQ system (right).*

7.6.2 DAQ board

The new TRBv2 [86] was used for acquisition system (Fig. 7.43 sketches the main components of the hardware in the left side and the hardware itself in the right one), being designed at GSI as a general purpose trigger and readout board with on-board DAQ functionality. Four of these TRBs are needed to instrument a full RPC sector. Although the first version (TRBv1, see section 6.3) was designed to readout the HADES RPC detector [11], the second version has been thought in a way to be detector independent. To broaden the spectrum of possible applications in future DAQ-systems, a very high data-rate digital interface connector (15 Gbit/s) has been included. It gives the possibility to mount add-on boards to the TRBv2 which then provide the detector-specific interfaces (special connectors) or FEE (like ADCs) and additional computing resources (FPGAs). The TRB will support EPICS [94] to allow the integration into the HADES Slow-Control System.

TRBv2 includes the following new functionalities:

- Uses an ETRAX-FS processor [93] for DAQ and slow-control tasks, running Linux 2.6 kernel in the 128 MBytes of memory and is directly connected to the 100 Mbit/s Ethernet link. The integrated three co-processors (each 200 MHz) allow a high IO bandwidth without main CPU intervention.

- A large FPGA (Virtex 4 LX40 + 128 MBytes RAM) and a Tiger Sharc DSP (500 MHz, 24 MBit memory) can be used as on-board resources for trigger and on-line analysis algorithms.

- Provides an optical link with 2 Gbit/s connectivity, serialized by the TI TLK2501, as a replacement of the HADES trigger bus and for high speed data transport.

7.6.3 Experimental setup

Fig. 7.44 shows the experimental setup of this test. The RPC detector used is the prototype described in [34], having 186 individual 4-gap glass-aluminum shielded cells distributed in three columns and two layers, covering an area of 1.26 m^2. 162 cells, distributed in 27 rows, were readout by the FEE boards (12 MBOs and 96 DBOs fed by two LV boards [108]) and four TRBv2 [86]. The last four rows of cells at high polar angle region were not instrumented due to a problem with the short MBOs. Additionally, some of the electronic channels were not operative.

The RPC was operated with a gas mixture composed of 90% $C_2H_2F_4$ and 10% SF_6 (slightly different than the standard mixture [83]), at a nominal High Voltage of 5.8 kV. Data were taken with the detector exposed to secondaries from reactions of a ^{12}C beam of 2 AGeV, with an effective spill duration of ∼6 s, on Nb and Be targets. A detailed description of the structure can be found in Ref. [34]. It was mounted on its support (Fig. 7.44) and placed approximately at the nominal position, between the Pre-Shower [18] (RPC downstream) and the MDCs [13] (see Fig. 2.1).

The last outer MDC (MDCIV) and the the Pre-Shower detector of the same sector were operational, allowing the external measurement of the particles through the timing RPC wall. The magnet and the RICH [15] were off. In order to provide a reliable reaction trigger, we operated the present TOF and TOFino walls [17] of the remaining sectors with a low-bias trigger in multiplicity N_i>4 ($\langle N_i \rangle \simeq 10$). We also ran low statistic triggers with two reference scintillators as in Ref. [65].

7.6.4 Measurements

Definition of the reference tracks and alignment

A set of reference tracks was defined as those tracks that matched both the MDC tracking system and the Pre-Shower detector within a window of ΔX_{match}=±35 mm in X (along the azimuthal angle) and ΔY_{match}=±35 mm in Y (along the polar angle). Due to the non-standard position of the RPC, a few centimeters backwards from the nominal position, it was necessary to make a careful alignment. This was done by minimizing differences between the position of the reference tracks on the RPC plane and the position given by the RPC itself, X_{res} and Y_{res}. The RPC hits were associated with a given tracks choosing the one at the minimum distance R_{res}, defined as $R_{res} = \sqrt{X_{res}^2 + Y_{res}^2}$. The procedure can be summarized as follows:

- X and Y position of a reference track given by the RPC was calculated as:

$$X_{rpc} = \frac{t_l - t_r}{2} v_{prop} + X_{offset} \tag{7.4}$$

  where t_l and t_r are the measured times left and right for each cell, v_{prop} is the signal propagation velocity in the cell and X_{offset} is an offset calculated individually for each cell. Y_{rpc} was calculated as the center of the hit cell obtained

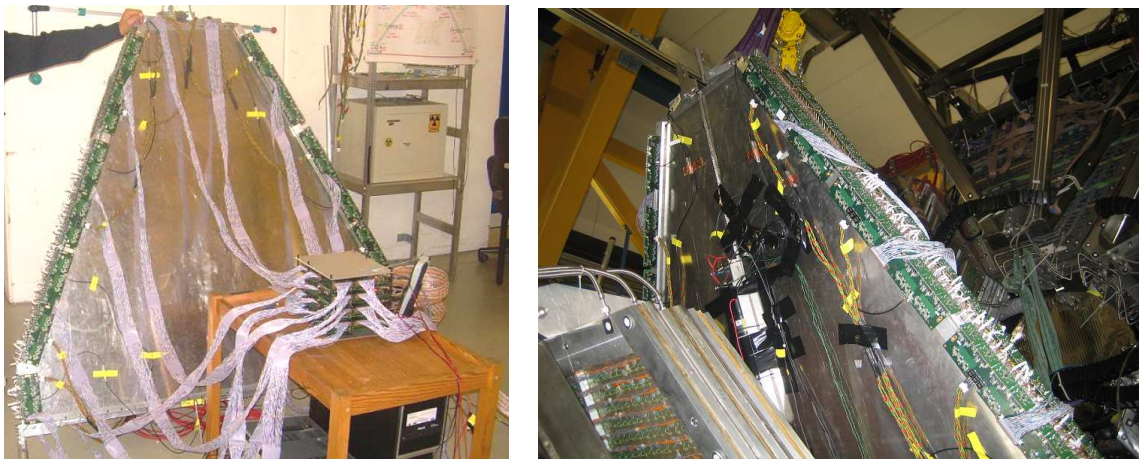


Figure 7.44: *Experimental setup of the RPC sector before (left) and after (right) the first installation in the HADES spectrometer.*

from its physical position. The propagation velocity v_{prop} was calculated with Eq. 7.5, where $W(t_l - t_r)$ is the width of the distribution of $t_l - t_r$ and D is the physical dimension of the cell:

$$v_{prop} = \frac{2D}{W(t_l - tr)} \tag{7.5}$$

- The RPC was aligned by centering and minimizing the rms of the X_{res} and Y_{res} distributions. The free parameters in this procedure are Z (RPC position downstream along the sector rails), Y (RPC position along the polar angle) and Θ (angle that quantifies the deviations from the perfect parallelism with respect to the Shower detector). The other three free parameters needed for positioning a volume in space were assumed to be fixed for the sake of different symmetries.

- After the alignment procedure, the propagation velocity was recalculated correcting the remaining residual dependence of X_{res} with X. Small deviations from the previously obtained value were identified and corrected.

Matching and intrinsic efficiencies

The matching efficiency is obtained on a given region as the ratio of the number of RPC hits, with in a position window ΔY=±35 mm and a time window ΔT=400 ns, and the number of reference tracks. T represents the time respect to the trigger signal given by the TOF+TOFino wall (no start detector were available). This time does not represent a time of flight but can be used to suppress random matches.

The intrinsic efficiency is calculated as the fraction of RPC hits in coincidence with the scintillators in a time window of 400 ns.

Intrinsic spatial resolution

The intrinsic spatial resolution is calculated for those tracks that cross two overlapping cells by obtaining the σ of the distribution:

$$\Delta X_{up-down} = \frac{v_{prop}}{2}[(t_l - t_r)|_{up} - (t_l - t_r)|_{down}] \tag{7.6}$$

where *up* and *down* denote the two overlapping cells placed on different layers. Assuming equal resolution for both cells, the spatial resolution for a single cell is σ_x=$\sigma(\Delta X_{up-down})/\sqrt{2}$.

For those cells that geometrically overlap with two cells (see an extensive geometrical description in [22]), the distribution of $\Delta_{up-down}$ is merged together and the σ_x of the resulting distribution is calculated. A similar procedure is used to calculate the average spatial resolution of the full sector or for a interest region.

Time resolution

The electronics tests have been performed using narrow test pulses that were sent from the TRB to the FEE. We measured the time resolution of the whole electronic chain as the width of the time difference distribution between two channels.

The time resolution is calculated for those tracks that across two overlapping cells by characterizing the distribution of Eq. 7.7 [11].

$$\Delta T_{up-down} = \frac{(t_l + t_r)|_{up}}{2} - \frac{(t_l + t_r)|_{down}}{2} \tag{7.7}$$

In order to characterize the resulting non-Gaussian distribution, the σ of a Gaussian fit within $\pm 1.5\sigma$ about the mean of the original distribution, $\sigma\Delta T_{up-down}|_{\pm 1.5\sigma}$, as well as the amount of events beyond $\pm 3\sigma$ (3-σ tails) were calculated. Assuming the same resolution for both cells, the time resolution for a single cell is σ_T=$(\sigma\Delta T_{up-down}|_{\pm 1.5\sigma})/\sqrt{2}$. This distribution is calculated after performing two corrections, as a function of position and charge. For cells overlapping with other two and for regions of interest, a similar procedure as described above is used.

Dependence on rate

A few runs were taken at different beam intensities. Moreover, as the rate within the sector varies exponentially as a function of the polar angle, it is possible to measure different rate values on the RPC for the same run.

Cells were grouped in six regions, with equal number of events, along the polar angle. For each region, the rate was calculated as the average rate in the region, the time resolution was calculated as the σ_T of the merged distributions of $\Delta T_{up-down}$ for the cells in the region and the matching efficiency was calculated as the average of the matching efficiency in the region. The intrinsic efficiency is just calculated for the available runs at different rates.

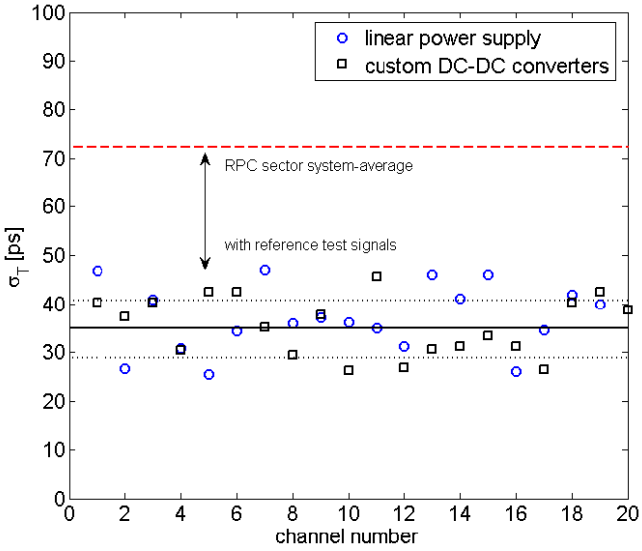


Figure 7.45: *Time resolution for two random samples of 20 FEE channels when using linear power supplies (circles) and custom DC-DC boards (squares). Average value (continuous line) and ±RMS (dotted) of the custom boards is also shown. The average RPC time resolution for a full instrumented sector [107] is indicated with a dashed line.*

7.6.5 Results

Time resolution

One of the most important aims of this test was to analyze the stability of the whole system (RPC, FEE and DAQ) with the new LV boards, together with the time resolution of the whole chain. A full sector was assembled and operated with linear power supplies, obtaining an average time resolution σ_T=35 ps measured with the TRB, being T=1/2($t_{left} + t_{right}$) the mean time between two FEE channels (Fig. 7.45), obtained with reference test signals. This resolution accounts for the resolution of the full electronic chain at fixed input amplitude (Q>100 fC).

Under the same conditions, the linear power supplies were replaced by the 48 V power supplies and LV boards, obtaining similar performances. This picture also shows the average value (continuous line) and ±RMS (dotted) of the boards, together with the average overall time resolution of the system of 73 ps [107]. The average time resolution of the FEE only (DBO+MBO) is 15 ps/channel σ, measured with a digital Tektronix oscilloscope TDS6154C Series (featuring 15 GHz bandwidth). The threshold was set at -10 mV for all channels.

The present system has been successfully used in-beam for powering one detector sector. Figure 7.46 shows the $\sigma\Delta T_{up-down}$ distribution for the whole system using Eq. 7.7 before and after the slewing correction. The inset picture corresponds to the case before the correction, showing a time resolution σ_T=106 ps σ per detector.

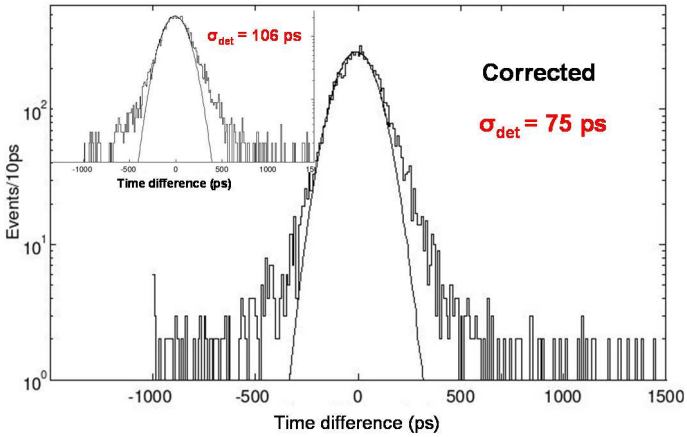


Figure 7.46: *Time resolution of the whole chain RPC+FEE+TRB, showing a σ_T=75 ps/channel after position and charge corrections.*

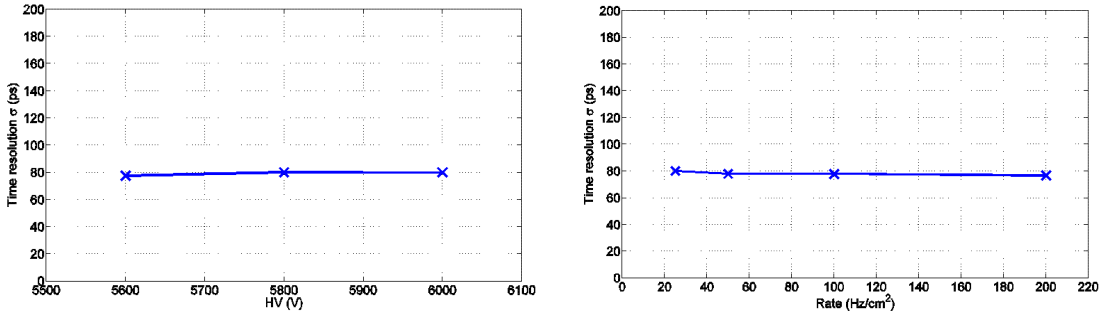


Figure 7.47: *Time resolution as function of the High Voltage (left) and the rate (right) during first installation in HADES.*

In this measurement we applied two different corrections: the position and the charge (slewing) corrections [34], showing an improvement σ_T from 106 to 75 ps per detector. Tails are also reduced from 2.5% to 2.2% above 3σ. The partial overlap of the layers completely eliminates longer time tails for a large fraction of the hits [75]. The threshold was set at -50 mV for all channels and not significant differences were observed changing thresholds regarding the time resolution measurements.

Figure 7.47 shows the time resolution σ_T of a single cell as function of the High Voltage applied to the cells (left) and the rate (right). Results corresponding to the HV show a constant value for range analyzed between 5600 and 6000 V. Results corresponding to the rate show also a constant value from 20 up to 200 Hz/cm^2. In both cases, the time resolution σ_T is below 80 ps.

The upper part of Fig. 7.48 shows σ_T as a function of the row number and Y for left, center and right columns. There are two regions clearly identified for rows higher and lower than 20, the latter being characterized by non-perfect shielding of the signal-feed-through, which results in a higher level of crosstalk by roughly a

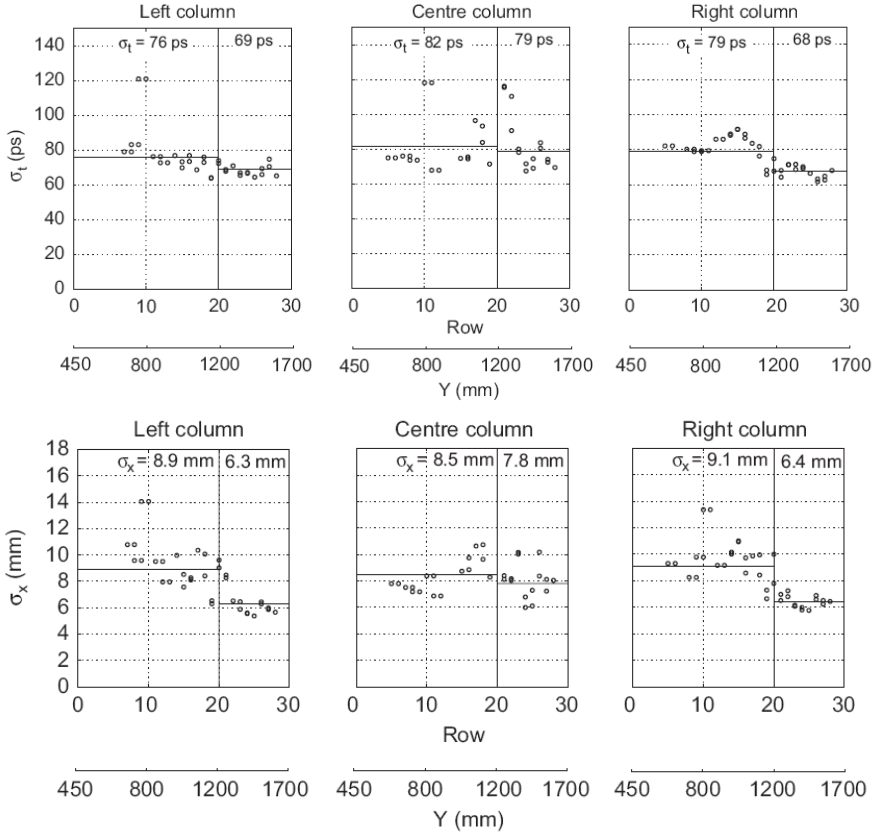


Figure 7.48: *Up: time resolution as function of the row and the Y-coordinate. Down: the same for the position resolution, both during the HADES installation.*

factor 3 [34]. The difference is clear, mostly on the lateral columns. Although the worsening is not dramatic, it is consistently at a level of 10 ps (the upper numbers on each plot denote σ_T of the merged distributions for the cells belonging to each region separated by the vertical line). There are a few randomly positioned cells with clearly worse resolution σ_T >100 ps, some of them correlated with a degradation of the spatial resolution, directly depending on the FEE resolution. This behaviour will be solved on the final sectors by replacing the cells or the FEE channels involved.

Intrinsic spatial resolution

Figure 7.49 shows the X_{res} distribution for the reference tracks, within a ΔY window of ±35 mm, after RPC alignment. The σ of the distribution, including tracking and RPC resolution, is $\sigma_{X_{res}}$=10.2 mm.

The lower part of Fig. 7.50 shows σ_x as a function of the row number and Y for left, center and right columns. Rows lower than 5 are not shown because the sector was a few centimeters backward from the nominal position and this region was shaded by the frame of the tracking system. In addition, some cells were not available because the respective FEE channels were inoperative and to calculate position or time both

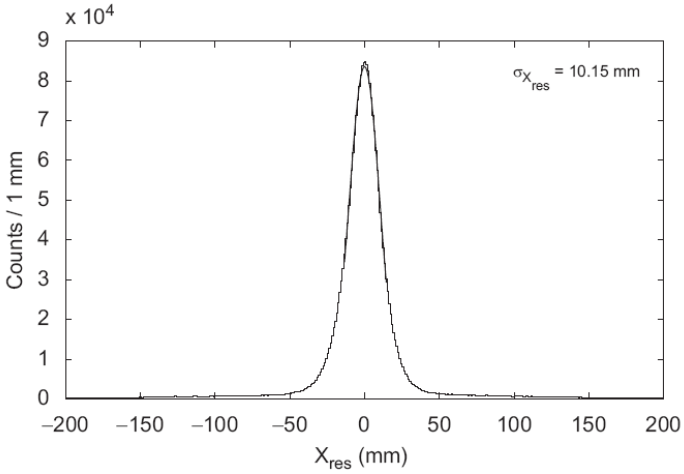


Figure 7.49: *X_{res} distribution for the reference tracks, after RPC alignment, showing a σ_x=10.5 mm.*

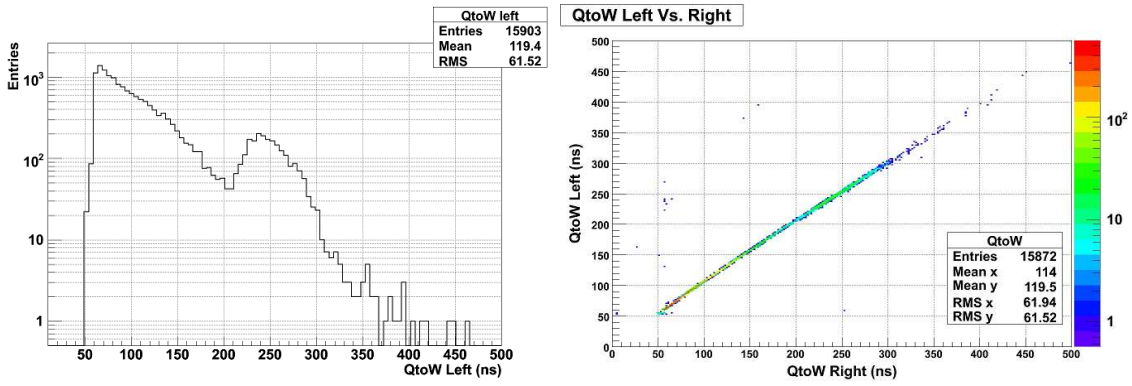


Figure 7.50: *Left: QtoW spectrum for the left side of one RPC cell. Right: QtoW of the right side vs. the left side of the same RPC cell.*

t_l and t_r of each cell are required. Again the difference between rows higher and lower than 20 is clear, mostly on the lateral columns. The difference, although not critical, is ∼2 mm (the upper numbers on each plot denote the σ_x of the merged distributions for the cells belonging to each region separated by the vertical black line). The global spatial resolution of the whole sector is 7.7 mm σ and compared with $\sigma_{X_{res}}$=10.15 mm, it suggests a good resolution of the tracking system as it is strongly influenced by the intrinsic spatial resolution of the RPC.

Charge-to-Width (QtoW) measurements

QtoW algorithm is needed for the slewing correction applied to time measurements. Figure 7.50-left shows a typical QtoW spectrum of the left side of one RPC. A clear structure appears for wider signals (QtoW>200 ns), corresponding to the streamer region. The charge and time information is measured twice at both sides

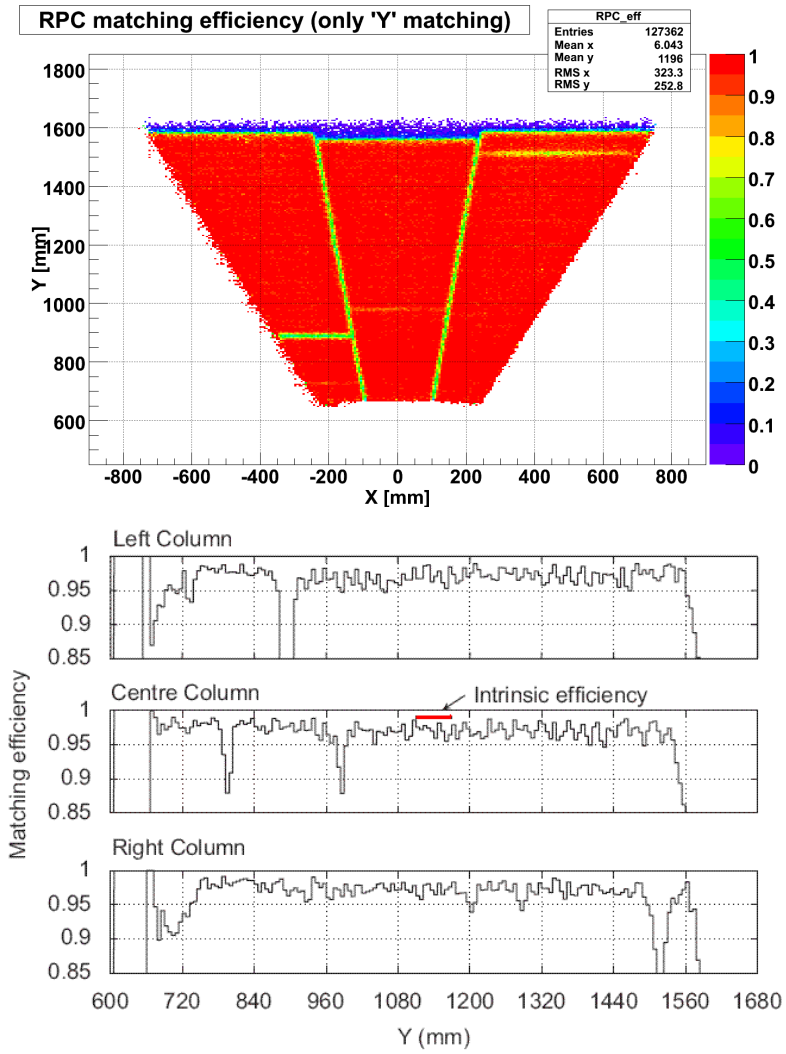


Figure 7.51: *Up: 2D matching efficiency scan. Down: 1D matching efficiency for the three different columns. The average values are 97.4%, excluding the non-operative channels. The intrinsic efficiency obtained with scintillators is 99%.*

of the cells. The plot shows that the ratio of streamers is around 10% of the events. Fig. 7.50-right shows the QtoW behaviour of one side vs the other from the same cell. The correlation between both sides shows a linearity, providing a minimum QtoW value of ∼50 ns, corresponding to the minimum charge of the RPC signals.

Efficiency

The upper part of Fig. 7.51 shows the 2D matching efficiency for reference tracks within a ΔY window of ±35 mm. The slanting lines separating the three columns are non-active regions in the RPC (counts in this region come from the imperfect resolution of the reference tracks).

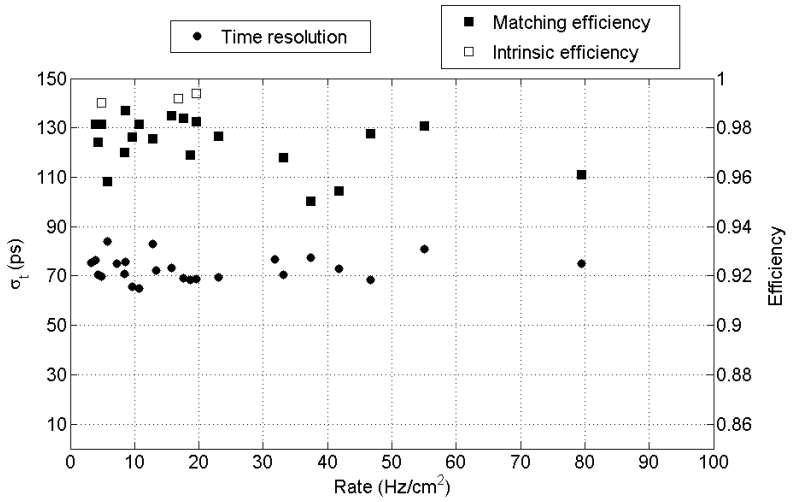


Figure 7.52: *Time resolution and efficiency as function of the rate during the first installation in HADES.*

The lower picture shows the 1D matching efficiency for each of the columns. The average efficiency is 97.4% (excluding non-operative channels). It also shows the intrinsic efficiency obtained with the scintillator for the same conditions (red short line at the middle of the center column) reaching a value of 99%.

Dependence on rate

Figure 7.52 shows the time resolution, σ_T, as a function of the rate, showing a constant value, within the available statistics, from a few Hz/cm^2 to almost 100 Hz/cm^2. The mean value of the data is σ_T=73 ps indicating that the parametrization procedure described in this section is very robust. Matching and intrinsic efficiencies are also shown at the same rates. The available values for the scintillator only reach 20 Hz/cm^2) showing constant values of 97.4% and 99%, respectively.

7.7 Conclusions

After the first installation of one full timing RPC sector, together with its FEE and DAQ systems, in its nominal position inside the HADES spectrometer and the good performances of the whole system regarding stability, time resolution and efficiency, we conclude to develop the final version of the FEE. New versions of both, DBO and MBO boards, were developed.

In the next chapter, the final version of the Front-End Electronics developed for the HADES tRPC wall will be presented, together with the commissioning of the full sectors and their final installation in HADES.

Chapter 8

Commissioning of the HADES RPC wall with final FEE version

8.1 Introduction

The final version of the Front-End Electronics (FEE) developed for the tRPC wall of the HADES spectrometer consists on two boards, the DBO and the MBO [56], having the same configuration than in previous STEP3 to STEP5 designs [80]. The acquisition system used together with the FEE is also based in the TRBv2 [86], the same used in previous tests (see chapter 7). The details are shown in Fig. 8.1, where a block diagram of the system FEE and DAQ is shown, including the connection between both systems.

Next section show the final version of the DBO and the MBO boards. Both designs are the upgrade of the previous DBO-STEP5 and MBOv2 (see chapter 7).

8.2 Final version of the FEE boards

8.2.1 The DaughterBOard design

The final version of the active DBO, the so-called STEP6, is a 4-channel 6-layer board of $5 \times 4.5 \approx 22.5$ cm^2, the same dimensions than previous versions. Fig. 8.2 shows both outer layers, TOP and BOTTOM, which allocate the electronic components. There are two different channels at each side of the board. The connection between the DBO and the RPC is also done through a RF connectors series MMCX, type Telegärtner J0134, the same as for STEP5 design (see section 7.2). Each one-channel female connector is mounted directly on the PCB of the cells.

In the design of the board (see Appendix B) the same special technical issues, used in previous designs, were required. For this purpose, the TXLINE programm is used to control the impedance of the paths and for impedance matching in PCB traces the stripline solution is also chosen (see Equations 6.1 to 6.4 of section 6.2).

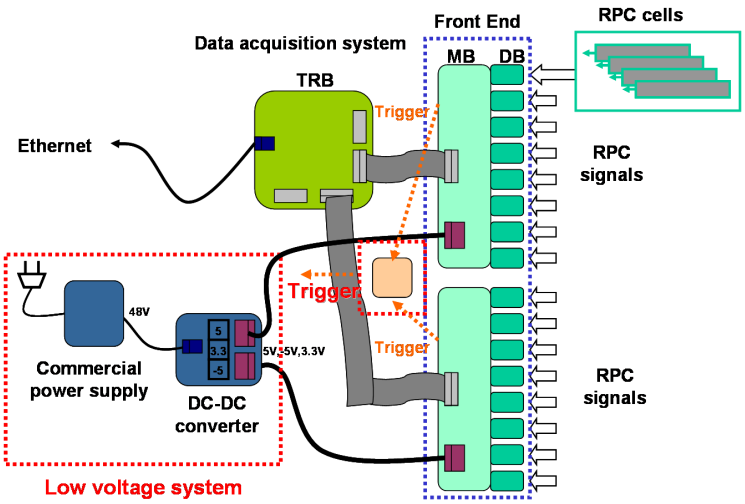


Figure 8.1: *Block diagram of the system FEE and DAQ of the RPC wall, where groups of four RPC cells are connected to one DBO, eight DBOs are connected to one MBO and, finally, four MBOs are connected to one TRB.*

The main features of the DBO-STEP6 are the same of the previous STEP5 design:

- One amplification stage with a factor of amplification $G{\sim}40$.
- One LVDS digital signal to measure both the time information and the charge through the 'Charge to Width' (QtoW) algorithm.

The block diagram of the STEP6 is shown in Figure 8.3, showing the analog and digital stages. The schematics and the layout are presented in Appendix B.

Analog part design

The analog part of the final version of the DBO is also based in the MMIC Philips BGM1013 amplifier used in STEP5 design, featuring 35.5 dB power gain at 1 GHz (31 dB flat gain up to 2.2 GHz), 4.5 dB noise figure at 1 GHz and high linearity (see section 7.2). This amplifier works with an input/output impedance of 50 Ω.

The main differences respect STEP5 design are the following:

- The coupling capacitors and the pull-up inductance of the BGM1013 are increased to 100 nF and 22 μH, respectively, to avoid the undershoot of the analog signal (see sections 7.5 and 7.6).
- A second 2.2 nF capacitor at the output of the BGM1013 is implemented to avoid noise effects at the input of the discriminator.
- The Philips BAV199 low-leakage double diode is included at the input of the amplifier to avoid from possible discharges coming from the RPC cells, protecting the BGM1013.

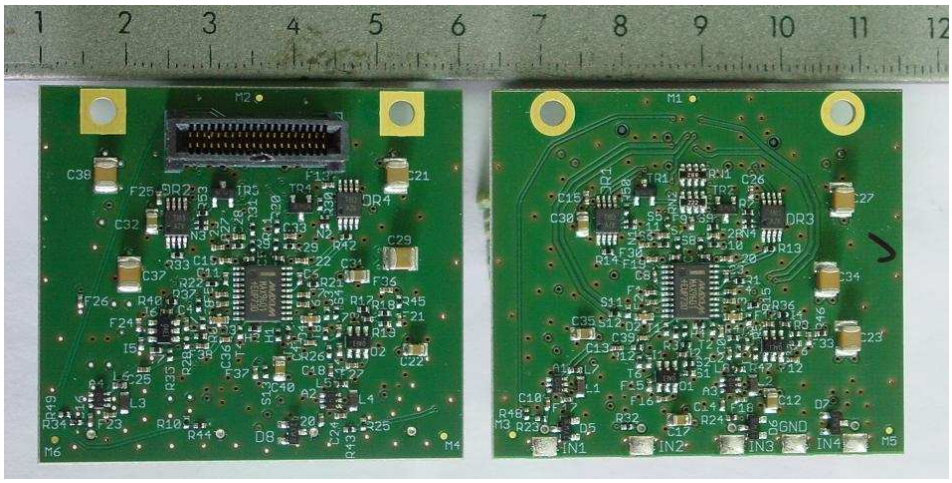


Figure 8.2: *Final version of the DBO with four channels per board. The size is 5×4.5 cm^2. The components are the same than in the STEP5 board, being placed in the same position (see Fig. 7.1).*

The output of the BGM1013 amplifier is split in two parallel branches, as in the STEP5: (a) an integration stage using the TI OPA690, a wide-band voltage-feedback operational amplifier, and (b) a dual Maxim ECL/PECL MAX9601 ultrahigh speed discriminator, where it starts the digital part of the design (see Fig. 8.3). The charge measurement is done through the 'Charge to Width' (QtoW) algorithm [56], as was described in the previous step.

Digital part design

The main differences regarding the previous STEP5 are the following:

- A voltage divider with 560-270 Ω resistors is included in the integration step at the output of the analog stage. The integration capacitor is increased by a factor 2 to 3.3 pF (increasing also the time constant), together with the RC constant of the $\overline{LE}$, giving a larger width at large pulse heights.
- A second 2.2 nF capacitor at the output of the amplifier stage is implemented to avoid noise effects at the input of the MAX9601 discriminator. The LE configuration is asymmetric and the RC constant of the LE is also increased.

The digital stage of the DBO-STEP6 starts with the same dual ECL/PECL MAX9601 discriminator (Fig. 8.3), featuring 500 ps propagation delay and ultrahigh speed. Two amplified output channels go to one dual MAX9601 for the timing (ToF discriminator with a positive threshold level). Positive RPC signals are required from the detector.

The latch enable of the discriminator provides the trailing edge of the digital signal when both signals cross each other. $\overline{LE}$ and LE are connected to the integrated

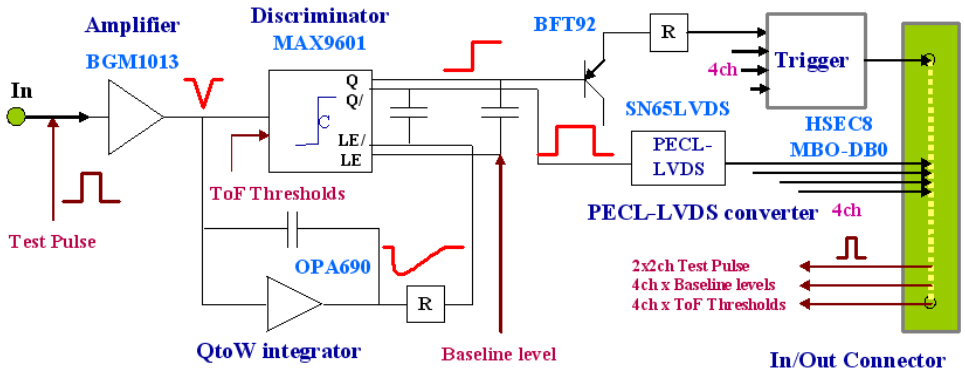


Figure 8.3: *Simplified block diagram of the final version of the DBO, showing all the important steps: amplification, integration and discrimination.*

signal and to an external DC level, respectively. The LE baseline can be adjusted and the output width can be controlled through the external DC level.

In the final DBO design the configuration of the latch enable is asymmetric: the output of the integrator is connected to the LE through a C=47 pF and this is connected to the external DC level and the $\overline{LE}$ is connected to the output $\overline{Q}$ of the discriminator through a C=27 pF, both connected through a 2.2 kΩ resistor [56]. In this way, the digital pulse encodes both the timing and the charge of the signals.

Finally, a TI SN65LVDS100 PECL to LVDS converter provides the LVDS signal required by the DAQ system. The DBO provides also a multiplicity signal to the HADES trigger unit through a sum of the channels of each DBO (with the same BFT92 transistor), which is sum again in the MBO.

8.2.2 The passive MotherBOard design

The MBO, developed by the IFIC group at Valencia, provides to the DBO:

- A stable and low ripple power supply voltage and ground.
- Programmable thresholds controllable via DACs.
- Test signals and paths for the readout of all the detector/trigger signals and temperature sensors.

The final version of the MBO (see Fig. 8.4) is an upgrade of the previous design presented in chapter 7. The MBO keeps the 32 channels per board in the same size (40×6=240 cm^2). The 32nd channel of each MBO is used for a reference time needed for the TRB. Due to space restrictions, a short version of the MBO housing only three DBOs (12 channels in 16.5×6.5 cm^2) has been made to instrument the wider part of the wall. MBO-TRB and MBO-DBO connectors are the same than were presented in sections 7.2 and 7.3 (see Table 7.1 and Fig. C.10 for the pin-out). Additionally, some features were improved respect to the previous MBOv2.

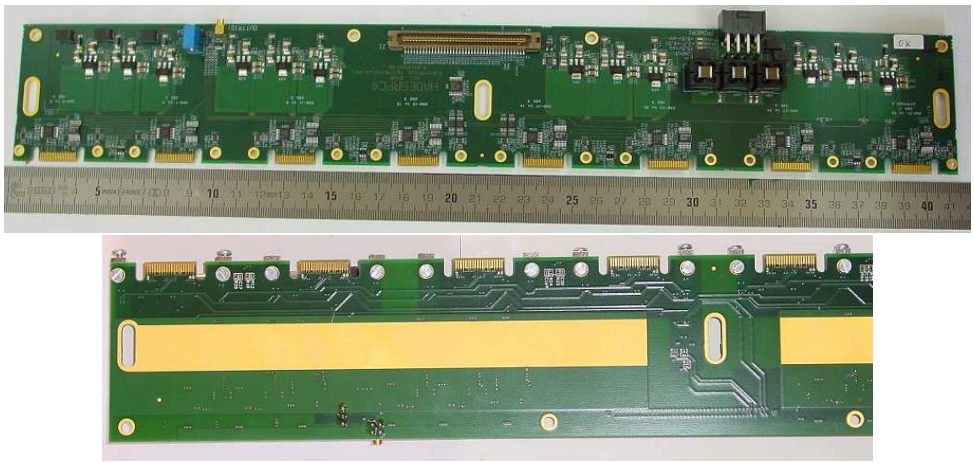


Figure 8.4: *Final version of the MBO with 8×4 channels per board, showing also the ground planes in the BOTTOM layer. The size is 40×6=240 cm^2. Components are the same than in MBOv2, being placed in the same position (Fig. 7.3).*

Grounding and stability

In order to improve the grounding connection and the stability of the FEE, a ground plane is included in the BOTTOM layer of the MBO (see Fig. 8.4). In this way, the contact between the FEE and the detector box is improved. Moreover, some filter capacitors are added in common mode to improve the power supply stability of the whole FEE system, also reducing the common mode noise [109].

Threshold voltages

In the new DBO design, the ToF thresholds required negative values. For this reason, a new inverters at the MBO level are added, the Burr-Brown for Texas Instruments 12 V and 7 MHz OPA4743 operational amplifier. Furthermore, an offset is added to the ToF threshold levels to have a positive value every time the system is started, avoiding the channels are firing. The defect value is 45 mV.

Low level trigger output

New resistors and capacitors values are needed at the summing stage in the MBO side. This is done to improve the behaviour of the trigger signal, eliminating the dependence of the baseline of the signal with the number of channels firing.

8.3 Stability test of the FEE final version

Before the commissioning of the RPC wall, a test of the final version of the FEE was developed at GSI (May 2008), in order to study the stability of the FEE assembled the same RPC sector used in the previous beam time (see chapter 7).

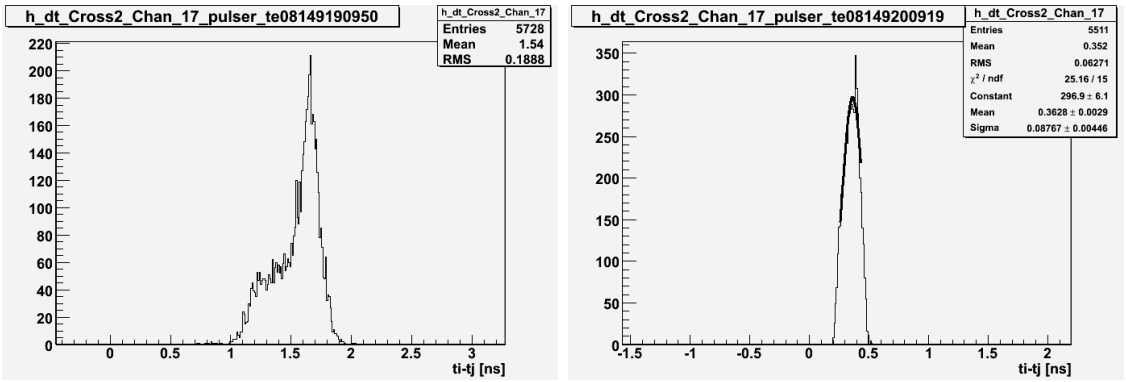


Figure 8.5: *$T_{left} - T_{right}$ of one cell measured with test signals, before (left) and after (right) removing the 68 Ω resistor at the test input.*

The experimental setup was the same we used during the first RPC sector installed in its nominal position in the HADES spectrometer (see section 7.6 and Fig. 7.44). The RPC detector used is the prototype described in [69]. The detector was used only in a passive way, to analyze the behaviour of the FEE. 16 MBOs and 108 DBOs were assembled and four TRBv2 boards [86] were used to readout the FEE. The FEE was fed by two low voltage boards [108].

8.3.1 Time and position resolution measurements

A problem was observed only when test signals are injected in the test input of the DBO channels. As was shown in Fig. 8.5, in the plot of the ΔX done as $T_{left} - T_{right}$, a double peak structure appears for some channels (in this case at the left side of the plot). The problem is also reflected in the time resolution measurements and the rms of the tof (rms_T), as was shown in Fig. 8.6. In both cases, the problem is observed in both left pictures.

The problem was analyzed and we observed that a 68 Ω resistor between the test input and ground forced a too hight current at the input of the preamplifier step. This resistor was removed in six DBOs connected to two miniMBOs and results are presented in the right side of both figures. Fig. 8.5-right shows how the 'double peak' structure disappears. The right pictures of Fig. 8.6 show the improvements in the rms_T and the σ_T of each channel. In the first measurement, the rms_T for the channels of the miniMBO changed to a mean value of rms_T from 200 ps to 40 ps per channel. In the second measurement, the time resolution for all the combinations changed between 35 ps$<\sigma_T<$65 ps per channel, improving the values obtained for original settings, which changed between 40 ps$<\sigma_T<$100 ps. All these results were obtained for all the possible combinations, between channels with the same and with different test signals.

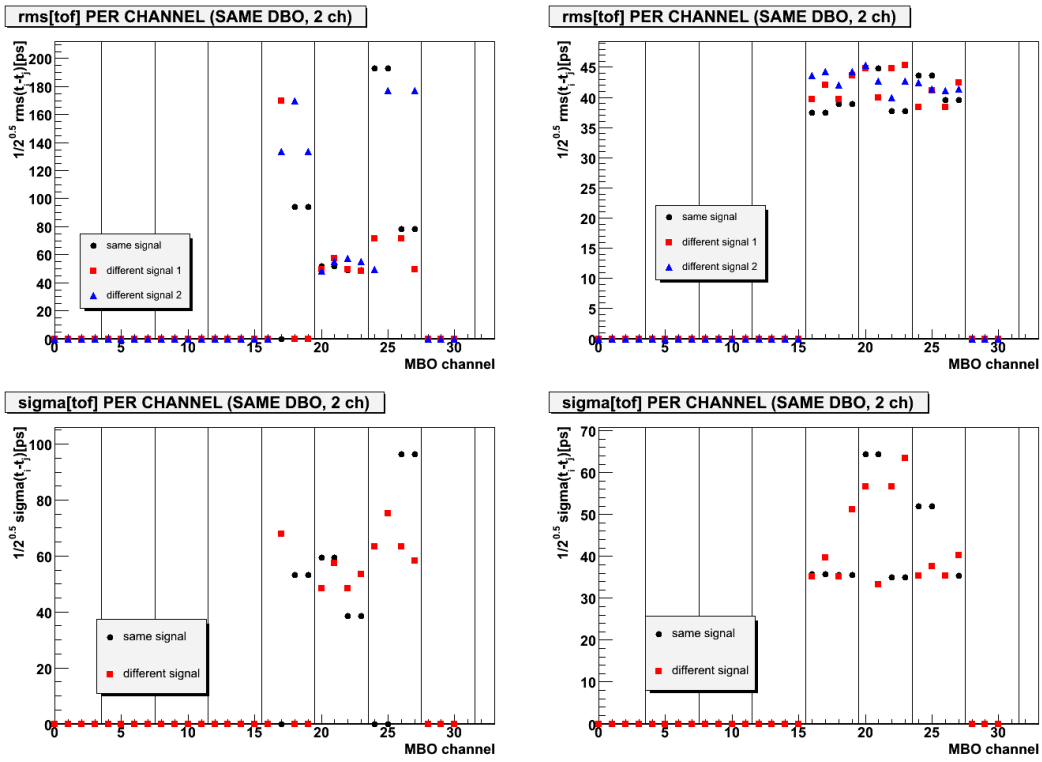


Figure 8.6: *Up: rms_T before (left) and after (right) the 68 Ω resistor was removed from the test input. Down: the same for the σ_T, showing the improvement after removing the resistor. Both measurements were done with test signals.*

8.3.2 QtoW measurements

The behaviour of the 'Charge-to-Width' algorithm (QtoW) implemented to measure the charge information was also studied. Two kind of measurement were developed to test the behaviour of the algorithm: both results are shown in Fig. 8.7.

The left picture shows the mean value of the QtoW output signal, obtained as a LVDS signal. The response to test signals has a constant value for all the channels, giving a mean value of ∼70±10 ps (more than a 95% of the channels have a value between 60 and 80 ps). The right one shows the rms of the QtoW measurement which gives the precision of the algorithm. The mean value is $rms_Q \simeq 200 \pm 50$ ps or lower for the 90% of the channels.

8.3.3 Cosmic rays test

Taking advantage of the current setup, a setup with cosmic rays was implemented to verify the FEE and detector behaviour, comparing the results with the ones of the previous beam time (Oct07) [107], [56].

The HV of the cells was set to 5730 V on both layers and the FEE ToF thresholds were set to -30 mV for all channels. The sector was mounted at its nominal position,

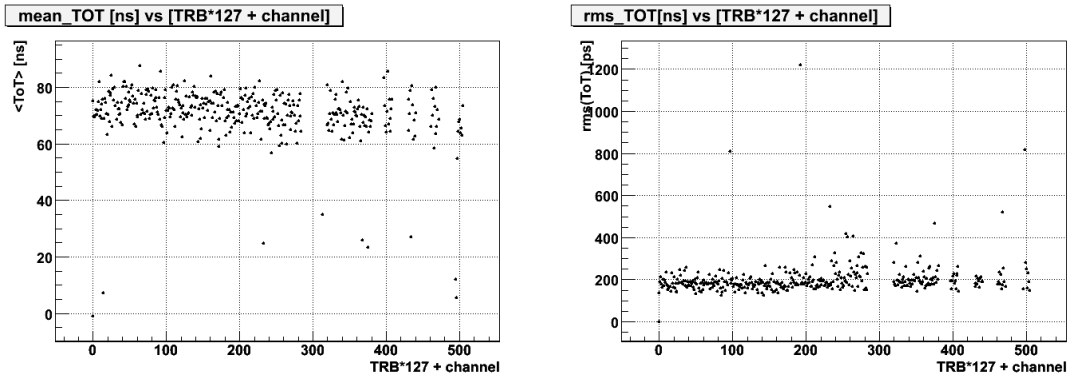


Figure 8.7: *Left: mean value of the QtoW algorithm, showing a value of 70 ps. Right: rms_Q, showing a mean value of ∼200 ps, except for wrong channels.*

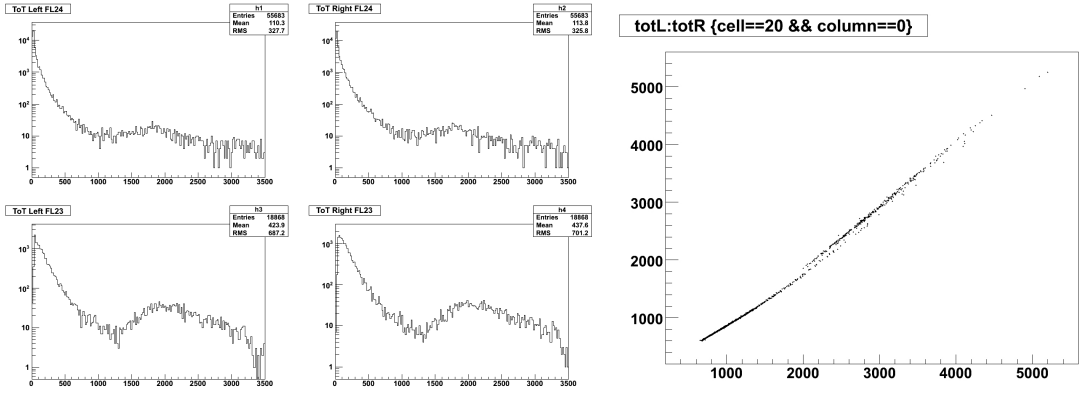


Figure 8.8: *Cosmic rays test with final FEE. Left: QtoW spectrum for two cells. Right: QtoW left vs right, showing a slightly different behaviour at high charges.*

being instrumented with the final FEE version, with the TOFino above it to be used as external trigger. The script used to analyze the data is the same that was used to analyze time and intrinsic spatial resolution from the beam run of Oct07.

Results seems to be basically the same compared with the ones from previous beam time. Differences are listed below:

- The charge measured at both sides (right and left) of a given cell is the same (see Fig. 8.8-left). In the previous data, the charge measured at both sides was different for some cells [56]. There are still a small difference for some channels, mainly at high charges (see Fig. 8.8-right), but they are not significative.
- The charge correction has changed, being more important at low charges. This could be because the threshold is lower compared with the beam time (-50 mV) or the charge spectrum for the cosmic rays (MIPs) is different, giving a different correction. As the cosmic rays have different angles (see Fig. 8.9) they could cross different number of gaps on each cell or even induce less charge.

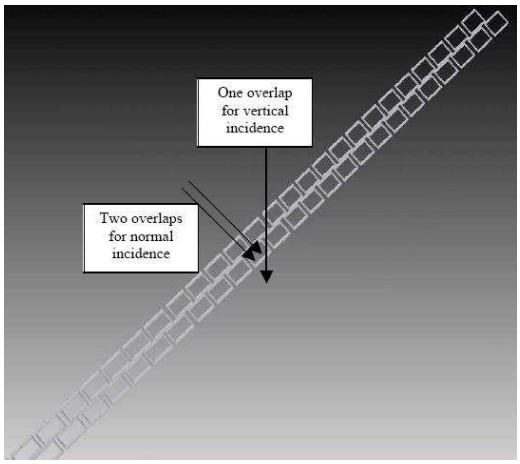


Figure 8.9: *Different incidence direction of the cosmic rays over the RPC box.*

- The time resolution is shown in Fig. 8.10. The red points correspond to the cosmic ray test [107], while the black points are from the beam time analysis (see section 7.6 and Fig. 7.48). There are more black points than red because on the data from the beam there are two available overlaps for each cell (n with n and n with n+1) while on the cosmic ray data there is only one (n with n+1). There is a residual number of coincidences on the neighbouring cells (n and n+2) but the resolution between them is worse (see Fig. 8.9).

  Fig. 8.10-up shows that the resolution is a few ps worse than in previous beam time. This can be explained taking into account Fig. 8.9: the cosmic rays can go through a few gaps only (not four) which could degrade the resolution. The region of non crosstalk is not clearly differentiated as on the beam data. Central columns above row 21 seem to be worse (but they were worse already).

- The intrinsic spatial resolution is shown on the lower plot of Fig. 8.10, being superimposed with the data from beam [107]. The behaviour is quite different although the values are similar. The region of non-crosstalk is worse that the crosstalk region, having a clear systematic worsening of the resolution for the bigger cells. We tried to select events with multiplicity one to verify if particle showers could eventually create multiple hits, which will affect more the bigger cells (bigger area) and would make the spatial resolution worst. But the effect was still there after this selection. This effect could be explained through the cosmic rays behaviour at high angles on the longitudinal dimension of the cells.

8.3.4 Conclusions

This test has validated the final FEE design for the RPC wall. A bug in the test input of the DBO was found and solved, replacing the 68 Ω resistor to ground for a 680 Ω, which reduces the current required and provides bigger test signals.

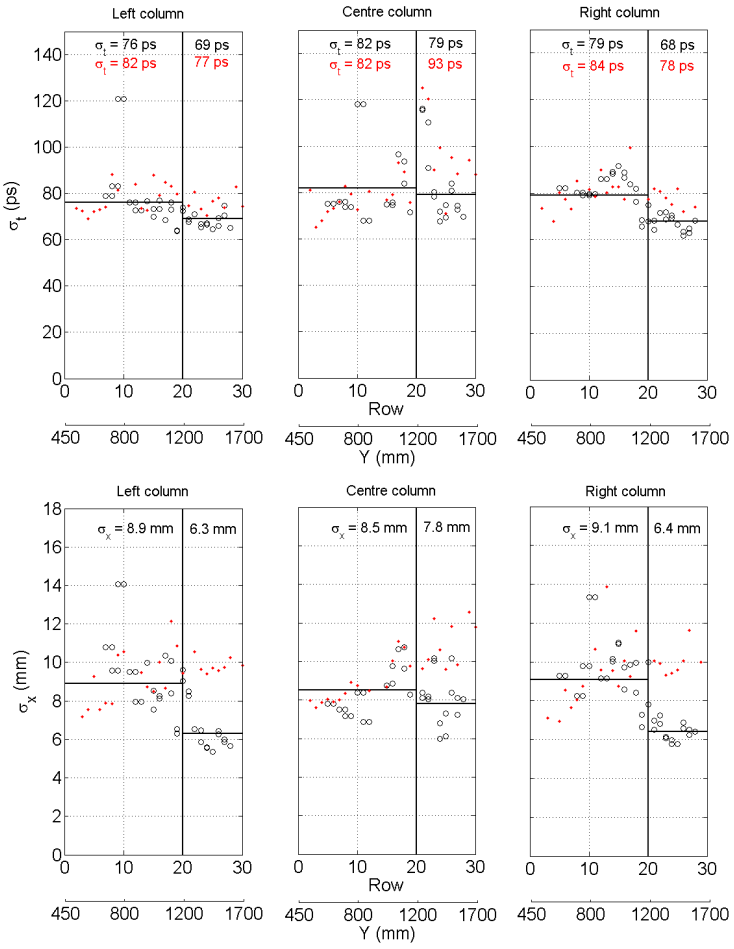


Figure 8.10: *Time (up) and position (down) resolution vs row for all the cells, comparing results of the cosmic run (●) and the previous beam time (○).*

Regarding cosmic rays test, results are quite similar to previous beam time ones, giving green light for the FEE mass production. This FEE design is the version we will assemble in all the six detectors which are part of the HADES RPC wall.

8.4 QtoW calibration

The electron induced (prompt) charge q_p was codified in the width of the FEE (LVDS) output signal through a 'Charge-to-Width' algorithm [56], that will be referred as QtoW. A calibration of the method to know the equivalence between the width in ns and the charge was done in two ways [110], using:

1. An external pulse generator, making measurements at several points of the DBO (input/output of the amplifier, integrator and discriminator, Fig. 8.11).

2. Real RPC signals.

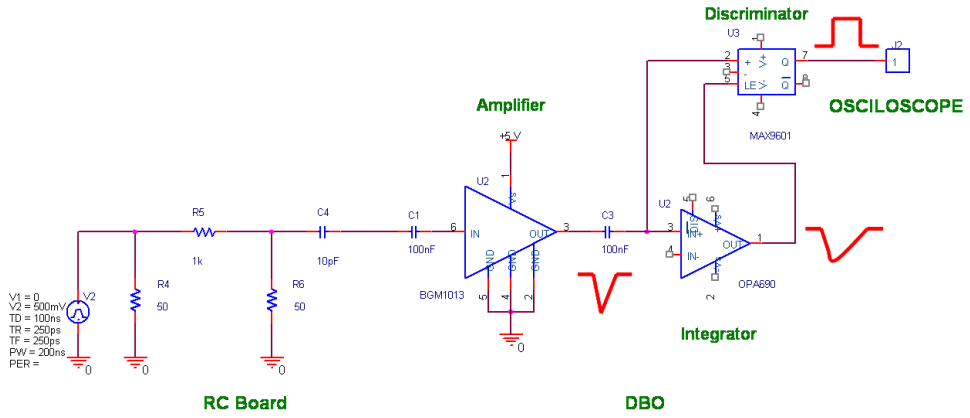


Figure 8.11: *Schematic of the RC board used for the QtoW calibration to simulate RPC pulses.*

8.4.1 Experimental setup

Figure 8.11 presents the experimental setup used in this test. For the measurements with the external pulse-pattern generator (the AGILENT 81130A series with 2 channels of 660 MHz bandwidth) we used a RC board with a voltage divider of a factor 20 and a 10 pF capacitor to inject signals similar to the RPC ones.

We measured the amplitudes and the charges at different points of the DBO: the input/output of the BGM1013 amplifier and the OPA690 integrator, respectively, and the correlation between QtoW at the output of the MAX9601 discriminator and the charge at the input of the board. As well as this correlation, we wanted to check the linearity of the amplifier and the integrator in amplitude and charge.

The charge at the input of the RC board could be calculated supposing it was a Heaviside step function ($H(t)$), also called the unit step function at the input of the board. The capacitor is discharged in the rise-time of the signal in the next way:

$$Q = V_{max} \times e^{-t/ZC} \tag{8.1}$$

where Z is the impedance and, if ZC$\gg t_{rise}$, the charge is:

$$Q = C \times V \tag{8.2}$$

In our board, Z=50 Ω and C=10 pF, giving ZC=500 ns. The input charge was injected using a fast square pulser (t_{rise}=0.35 ns and a width of 3 ns) through a differentiation board (C=20 pF, R=50 Ω) in order to emulate the shape of the RPC signals. Then, with Equation 8.2 we calculate the theoretical value of the charge injected at the input of the amplifier. We verified this value measuring this charge with a Tektronics TDS7104 Oscilloscope (BW=1 GHz), being the charge:

$$I = \frac{V}{Z} \Rightarrow Q = \int Idt = \int \frac{V}{Z} dt \tag{8.3}$$

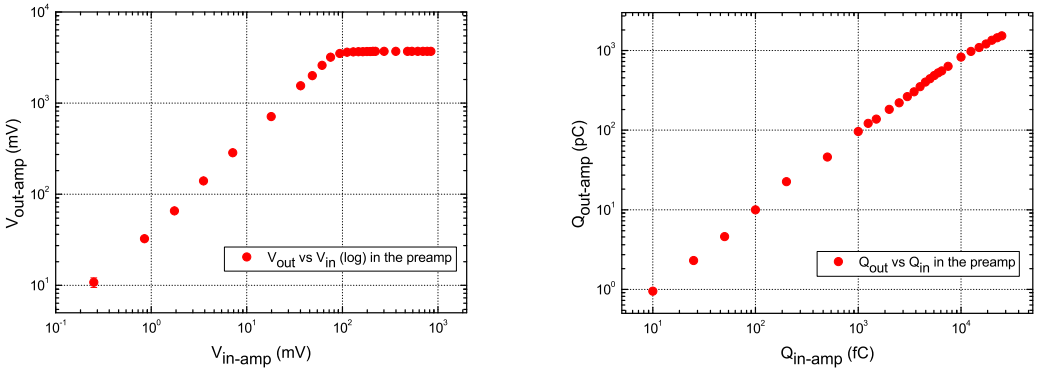


Figure 8.12: *V_{out} vs V_{in} (left) and Q_{out} vs Q_{in} (right) for the BGM1013 amplifier, both done with a pulse generator. It shows a linear behaviour in both cases, except for the amplitude which saturates the amplifier (for A>100 mV at the input).*

The charge is calculated through the area of the signal:

$$Q = \frac{\mu_T}{Z} \qquad [Coulombs] \tag{8.4}$$

and the total area of the signal is calculated as the difference between the area of the signal and its pedestal:

$$\mu_T = \mu_S - \mu_P \Rightarrow Q = \frac{\mu_S - \mu_P}{Z} \tag{8.5}$$

where the pedestal is calculated through a fixed time as:

$$\mu_P = \int baseline\, dt \tag{8.6}$$

8.4.2 Results with pulser and RPC signals

We measured the amplitudes at the input and output of the amplifier and the integrator, the charge in the same points, the input charge measured using Eqs. 8.5 and 8.6 and the width of the LVDS signal. The theoretical input charge was also calculated with Eq. 8.2 and compared with the charge measured with the scope.

Amplitude and charge correlations

Figure 8.12 shows the input/output correlations between the amplitudes and the charges of the BGM1013 amplifier. The left picture presents the behaviour of the amplitudes, showing a good linearity before the amplifier saturates in amplitude (for A>100 mV at the input). The amplifier has a factor gain of $G{\sim}40$, according with a 31 dB flat gain up to 2.2 GHz. The right plot presents the behaviour of the charge of the amplifier. The output charge as function of the input one shows a linear behaviour in all the range, with a smooth change for bigger charges (for Q>10^4 fC at the input), due to this saturation effect. But this effect is not important.

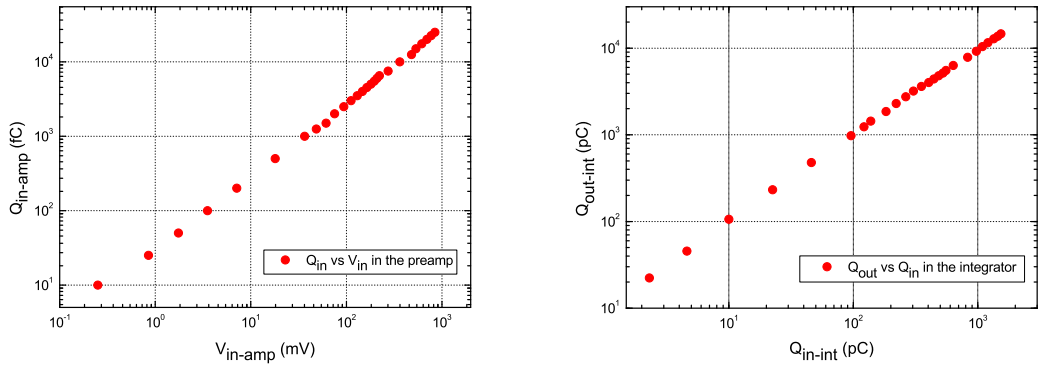


Figure 8.13: *Left: Q_{in} vs V_{in} for the BGM1013, giving the equivalence of the 'physical threshold' in charge units (∼30 fC). Right: Q_{out} vs Q_{in} for the integrator, showing a linear behaviour. Both measurements were done with a pulse generator.*

Fig. 8.12-left gives us an idea of the 'physical threshold' of our FEE. Taking into account the gain of our amplifier and the ToF threshold of the discriminator, the physical threshold of our FEE is ∼1 mV, obtained through next equation:

$$physical\,threshold = \frac{threshold}{gain} = \frac{50}{40} = 1.25\ mV \tag{8.7}$$

which is an important value to measure the sensibility of our electronics. This value is, for example, similar to the 1 mV obtained by the FEE of the ATLAS RPCs [111].

'Physical threshold' in charge units can be obtained plotting the Q_{in} as function of the V_{in} (see Fig. 8.13-left), where an amplitude of 1 mV corresponds to a charge of ∼30 fC at the input of the BGM1013 amplifier. This value corresponds to a RPC detector gain of $\sim 10^5$ [112]. A physical threshold of 30 fC is an optimum discriminating threshold for the HADES RPC cells, well above the 0.2 fC electronics noise level and much below the average fast pulse charges (around 1 pC, see Fig. 8.15-right), providing a large safety margin against system-generated noise or crosstalk from the neighboring cells.

Fig. 8.13-right shows the Q_{out} as function of the Q_{in} at the OPA690 integrator. The behaviour is linear in all the range, and not saturation effect is presented.

QtoW and charge correlations

After checking the linearity of the amplifier and the integrator, we analyze the behaviour of the 'QtoW algorithm'. The algorithm is non-linear as illustrated in Fig. 8.14, with avalanches lying mainly on a first (steep) linear part of the QtoW vs q_p correlation curve, while streamers are concentrated in a second (soft) one. Despite the non-linearity, avalanches and streamers can be well resolved (see Fig. 8.15) and appear separated at around $q_p \simeq 5$ pC (QtoW=200 ns). The charge spectrum shown in Fig. 8.15-right is similar to other ones obtained with previous RPC prototypes [22]. This 'QtoW method' can indeed accommodate a very large dynamic range while

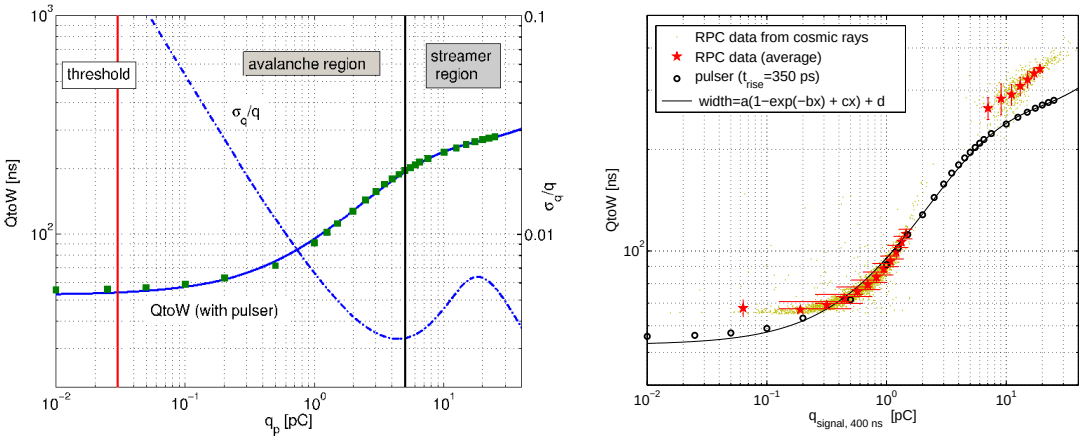


Figure 8.14: *Left: average behaviour of the output signal width (QtoW) as a function of the input pulser charge together with a 4-parameter fit. The avalanche and streamer regions are indicated and also the threshold level. The dot-dashed line shows the charge resolution resulting from the fit after including the fluctuations in the QtoW value (right axis). Right: the same behaviour of the QtoW, also including the charge of the RPC signals.*

keeping the charge resolution below 10%-σ for avalanche-like pulses with q_p>50 fC (see dot-dashed line at Fig. 8.14-left).

The bi-linear behaviour of the average signal width ($\overline{QtoW}$) as a function of the average prompt charge ($\overline{q}_p$) can be reproduced with the next parametrization [110]:

$$\overline{QtoW} = a(1 - e^{-b\overline{q}_p}) + c\overline{q}_p + QtoW_{min} \tag{8.8}$$

and the resolution of the 'QtoW algorithm' can be obtained:

$$\frac{\sigma_{q_p}}{\overline{q}_p} = \frac{\partial \overline{q}_p}{\partial \overline{QtoW}} \frac{\partial_{QtoW}}{\overline{q}_p} \tag{8.9}$$

$$\frac{\sigma_{q_p}}{\overline{q}_p} = \frac{1}{abe^{-b\overline{q}_p} + c} \frac{\partial_{QtoW}}{\overline{q}_p} \tag{8.10}$$

$QtoW_{min}$ (53 ns for the channel of Fig. 8.15-left) is the minimum output signal width, corresponding to the minimum time during which the comparator is being self-latched. By numeric integration of the signal amplitude, a close agreement for the QtoW vs q_p curves was observed when analyzing detector avalanches as compared with pulser data, while streamers clearly deviate from the pulser behaviour (up to a factor 1/2 less in the reconstructed q_p). The fluctuations of the signal width are of the order of σ_{QtoW}=200 ps and no dependence with the input charge was observed.

Next, we will try to explain the deviation observed for the streamers as compared with pulser results. The QtoW values of Fig. 8.14-left came from a pulse generator, while in the right plot, both pulser and RPC signals from a cosmic rays test are

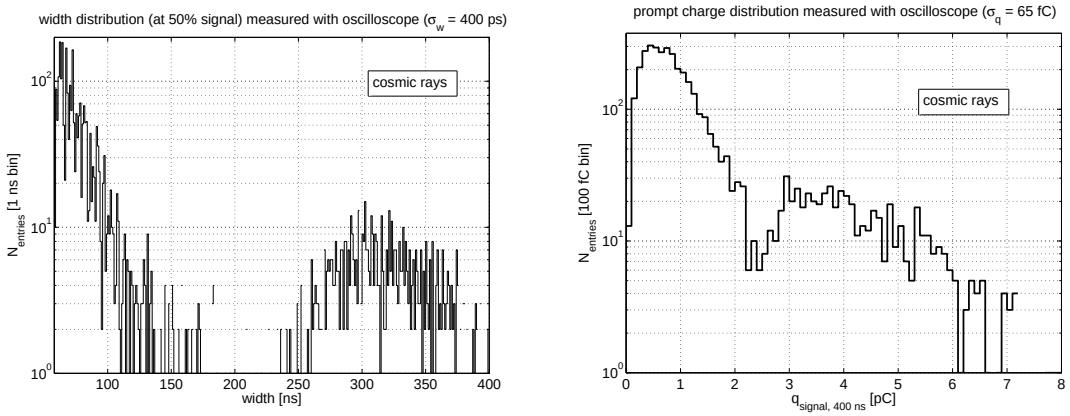


Figure 8.15: *Left: QtoW (left) and Q (right) spectrums, both obtained with cosmic rays during the QtoW calibration, both showing clearly the streamers region.*

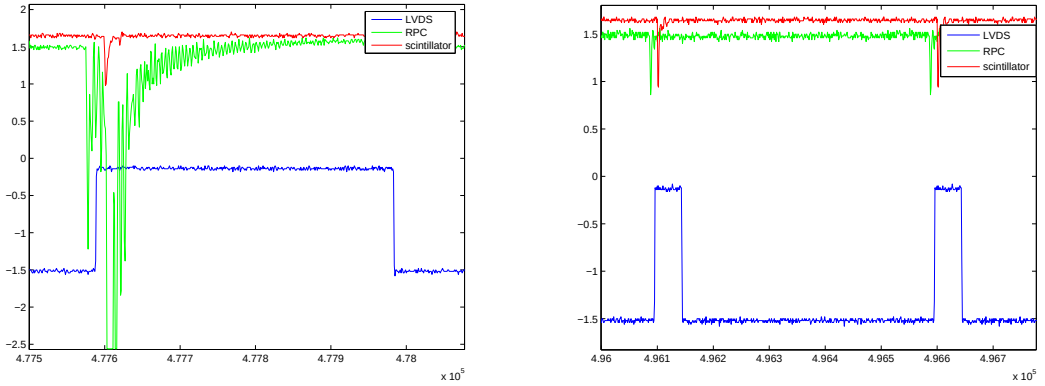


Figure 8.16: *Left: huge streamer, showing its typical ionic tail and a precursor. Right: two normal avalanche signals, both measured in the cosmic rays test.*

compared. Data from Fig. 8.15 come also from the cosmic rays test. As was pointed out, in the streamers region similar charge values corresponds to higher QtoW as compared with pulser ones. One explanation is that this effect is due to the ionic tail of the streamers which is bigger than for normal avalanches (see Fig. 8.16). Then, the width of the LVDS signal becomes higher for streamers. In signals coming from a pulse generator does not appear the ionic tail. Although the charge is the same, the QtoW is different, being bigger for charges distributed over time (with ionic tail) that if the charge is concentrated in one pulse. This could be because the $\overline{LE}$ discharge for signals with ionic tail is more flat and the crossing point between both LE signals, which give us the width of the LVDS signal, could change a few ns. This produces a bigger QtoW result for the streamers.

Eq. 8.8 provides an accurate phenomenological description and illustrates the different behaviour of the algorithm for low and high charges, but it cannot be inverted. So, in practice, a 5th order polynomial was used to obtain the 'calibration curve' $q_p(QtoW)$ (see Fig. 8.17). This curve was done for four different FEE channels

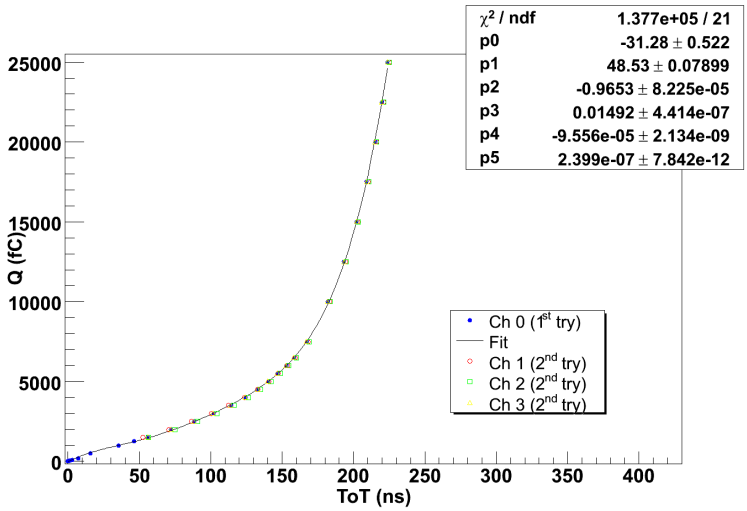


Figure 8.17: *Q as function of the QtoW done with pulser for four different channels, fitted to a 5th order polynomial function.*

placed in four DBO boards. The correlation is in good agreement for all of them after removing the QtoW pedestal of each channel. To avoid errors resulting from an incorrect extrapolation, values of the signal width in excess of 290 ns are considered as an 'overflow' and the maximum pulser charge of q_p=25 pC is assigned to them. Such big charges are rarely achieved under ordinary circumstances and they occurred seldom even in the very harsh environment studied here.

This calibration of the 'QtoW method' done in the LabCAF laboratory of the USC, together with a ^{12}C beam-time test developed at GSI with a few cells implemented with the final FEE version, are included in [110].

8.5 Production tests of the final FEE version

Some different tests were developed to validate the FEE channels of the final version to be mounted in the six RPC sectors in their nominal positions inside the HADES spectrometer. A total number of 756 FEE boards (including an extra sector, giving 3024 channels) were tested. The whole production of the boards was done during last months of 2008 and beginning of 2009. The tests started at the end of 2008, finished in summer 2009. However, the test of a pre-production representing about 5% of the whole production (30 boards) was performed at the end of 2008 to check the correct behaviour of the boards.

According to the production quality control procedures, a DC electrical test was performed before and after the assembly of the boards. The test is devoted to check the continuity of electrical lines, the power consumption and the voltage levels in input and output. Furthermore, a final AC test was performed in our laboratory, similar to the ones developed for the FEE of the ALICE RPCs [113], in order to

	Mean value ± Range	% of the total value
A_{ch} [mV]	400±20	10%
$A_{trigger}$ [mV]	45±5	22%
w_{ch} [ns]	200±10	10%
Δt [ps/channel]	<150+50	33%
σ_T [ps/channel]	16±5	∼33%

Table 8.1: *Parameters measured for the validation of the final version of the FEE, including the mean value with the acceptable range, together with the % of the total acceptable value in order to validate the channels.*

check the fully dynamical functionality of the 4-channel boards and to measure relevant electronics parameters through the output signals:

- The amplitude of the LVDS and the trigger signals (A_{ch} and $A_{trigger}$).
- The width w_{ch} of the LVDS signal, providing 'Charge-to-Width' information and the jitter in the measurement.
- Time resolution σ_T measured over the time difference between two channels.
- Crosstalk between different channel combinations.

For all these measurements we injected at the DBOs the test signals externally with a computer/software board developed by Dr. W. Koenig at GSI, featuring a CPLD[1] which is operated via four rotary switches. These board also allows to set thresholds and check the LVDS output signals which are sent to the same Tektronix digital oscilloscope used in previous tests. The power supplies were commercial ones. The value of the discriminator thresholds are relatively well peaked around the expected values. Channels with behaviours out of the requirements were rejected.

8.5.1 Measurements of different parameters

Amplitude of the LVDS and trigger signals

The amplitude of the LVDS digital output signals was measured and verified that the value was within a fixed range, being the amplitude 400 mV and the range:

$$A_{ch}=400\pm20 \text{ mV}$$

corresponding to a 10% of the total value (see Table 8.1). All the 3024 channels are inside this amplitude range, and any channel was rejected for this reason.

The amplitude of the trigger signal is generated in each DBO channel and it is summed at the MBO level for all the DBOs of each MBO (as was explained previously). Its amplitude is ∼45 mV per channel and the range chosen is:

[1]Complex Programmable Logic Device.

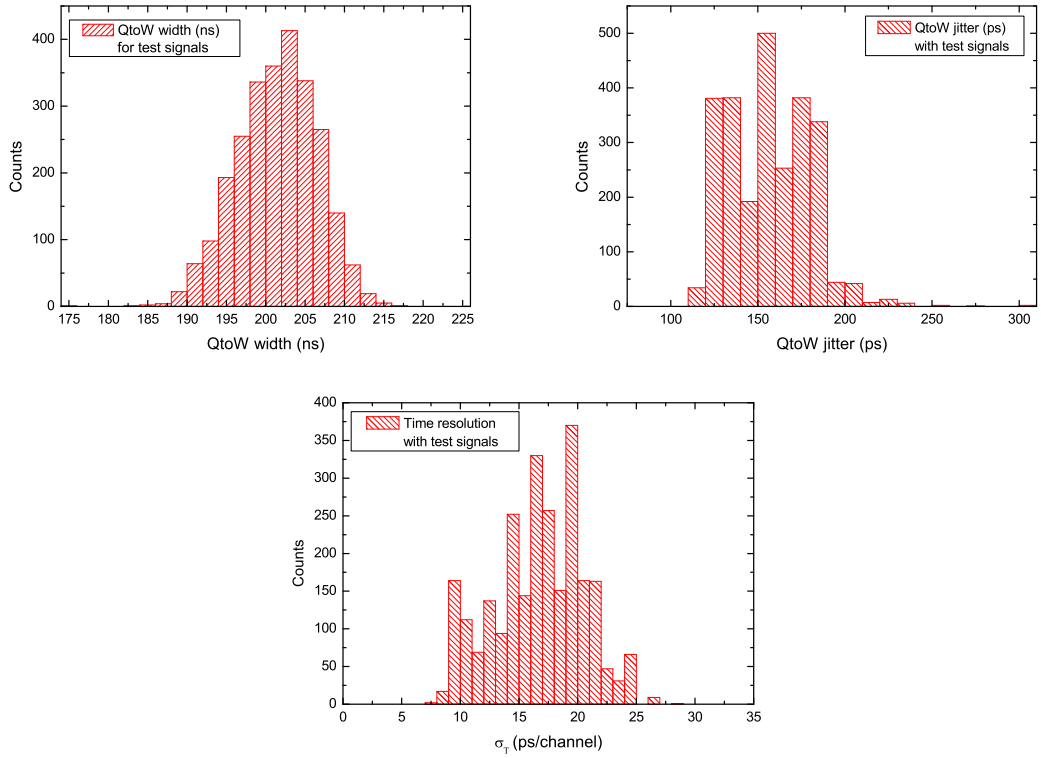


Figure 8.18: *Results with test signals corresponding to 648 DBOs (2592 channels) of the six RPC sectors. Up: LVDS output width (left), showing a mean value of w_{ch}∼200 ns and the jitter of the same measurements (right), showing a mean value of 150 ps (%0.1 of the total value). Down: time resolution per channel measured through several time differences, showing a mean value σ_T=16 ps/channel.*

$$A_{trigger}=45\pm5 \text{ mV}$$

corresponding to a 22% of the value and, as in the case of the LVDS amplitude signals, all channels had a correct behaviour.

Charge to Width algorithm

Two parameters were measured to validate the behaviour of the QtoW algorithm:

1. The width w_{ch} of the LVDS signals.

2. The jitter of the trailing edge of this LVDS signal.

The mean value of the LVDS width response to test signals is w_{ch}∼200 ns (see upper Fig. 8.18-left). The chosen range for correct channels, corresponding to a 10% of the total value, is:

$$w_{ch}=200\pm10 \text{ ns}$$

The mean value of the jitter of the width of the LVDS signal, which is a measurement of the resolution of the 'Charge-to-Width' method, is 150 ps (see upper Fig. 8.18-right). The accepted channels required a value of the jitter:

$$\Delta t < 150+50 \text{ ps}$$

corresponding to a 33% of the total value.

Time Resolution

The time difference between several combinations of two channels was also measured and adjusted to a gaussian fit to obtain the time resolution σ_T. The down picture of Fig. 8.18 shows the mean value of the time resolution, being 16 ps per channel (23 ps combined for two channels). The range for correct channels is:

$$\sigma_T < 16+5 \text{ ps}$$

corresponding to $\sim$30% of the total value. These results are summarized in Table 8.1.

Crosstalk between channels

Some tests were also done regarding crosstalk effects inside the FEE. With this purpose we injected an external pulse coming from a pulse generator (AGILENT 81130A pulse-pattern generator with 2 channels of 660 MHz bandwidth) at the input of one DBO channel. The fast signal tried to simulate an RPC signal and it was a 2 ns width pulse, with an amplitude of 20 mV and a rise-time of 0.3 ns.

In order to check if, decreasing the ToF threshold in the neighbour channels the discriminator fired at some level, this was done inside one board and also with all the eight DBOs of one MBO. Results show there is no crosstalk above 3 mV threshold and below this value it is very low, <1%. This crosstalk effect exists only between channels in the same DBO and no crosstalk was observed between different boards.

8.5.2 Summary of the validation tests

Over 3000 channels of the FEE were tested and main results are the following:

- Only 0.5% of the channels were not working (due to short-circuits, wrong behaviour, etcetera).
- 6.7% were working but with at least one parameter outside the limits (around half due to output signal width and half due to response time dispersion). This is not critical because in the RPC wall there are more FEE channels than cells.
- 92.8% were within specifications. This means that 2806 FEE channels are available for HADES RPC front-end boards production (while 2592 are needed). Then, we have enough channels to replace any possible board with problems.

- About 20% of the input cables of the DBOs have been replaced due to short-circuits between the grounding and the signal and wrong assembly of them.

Finally, the FEE developed for the RPC wall has been produced and tested. Their performances fulfills the HADES requirements, in terms of timing, charge and concerning the low threshold discriminator sensitivity.

8.6 Commissioning of the HADES-RPC wall

In April 2009, we started the assembly of the six timing RPC sectors with their corresponding FEE systems. At the beginning, the sectors were mounted in groups of two (two in April, two in July and the last two in October 2009) and validated with a cosmic rays test. At the end of the year, the full six sectors were assembled in their nominal positions in the HADES spectrometer. During 2010, the RPC ToF wall of HADES will be operative and different beam-times will be developed.

8.6.1 Temperature test of the FEE boards

Before the assembly of the second pair of RPC sectors done in July 2009, a temperature test of the FEE boards was developed. Both FEE boards, DBO and MBO, and their corresponding cables (RPC-DBO, MBO-TRB, and trigger cables) were subjected to an increase of temperature, trying to check the performances of the FEE boards and their soldiering points when we increase the temperature.

We have developed this test for all the FEE boards corresponding to one RPC sector: 12 MBOs, 4 miniMBOs and all the 108 DBOs, together with the corresponding cables. The test consisted in putting into the oven each single MBO with their DBOs, connected to one TRB to set the thresholds, send the test signals and acquire the LVDS output signals. It was done individually because there was not enough room inside the oven. Once the MBO was inside the oven we measured their performances. After this, we increased the temperature until 70 °C taking measurements every 10 °C. Finally, results for each temperature were compared. The upper limit temperature was 75 °C because some of the components of the FEE are specified for operation from -40 °C to 85 °C (the MAX9601 discriminator and the SN65LVDS100 PECL/LVDS converter).

The performances of the FEE boards and also the soldering points are not affected due to the increasing of the temperature until 75 °C. Figure 8.19 shows some results of this FEE temperature test as response to the test signals. The most important results show the similar behaviour of the time resolution σ_T and the rms_T between the channels of each single MBO while the temperature was increased. Results are presented for both the environment temperature ∼25 °C and 70 °C. Time differences between channels were done both for channels with the same test signals and with different ones (two and four measurements for each DBO, respectively). σ_T for the

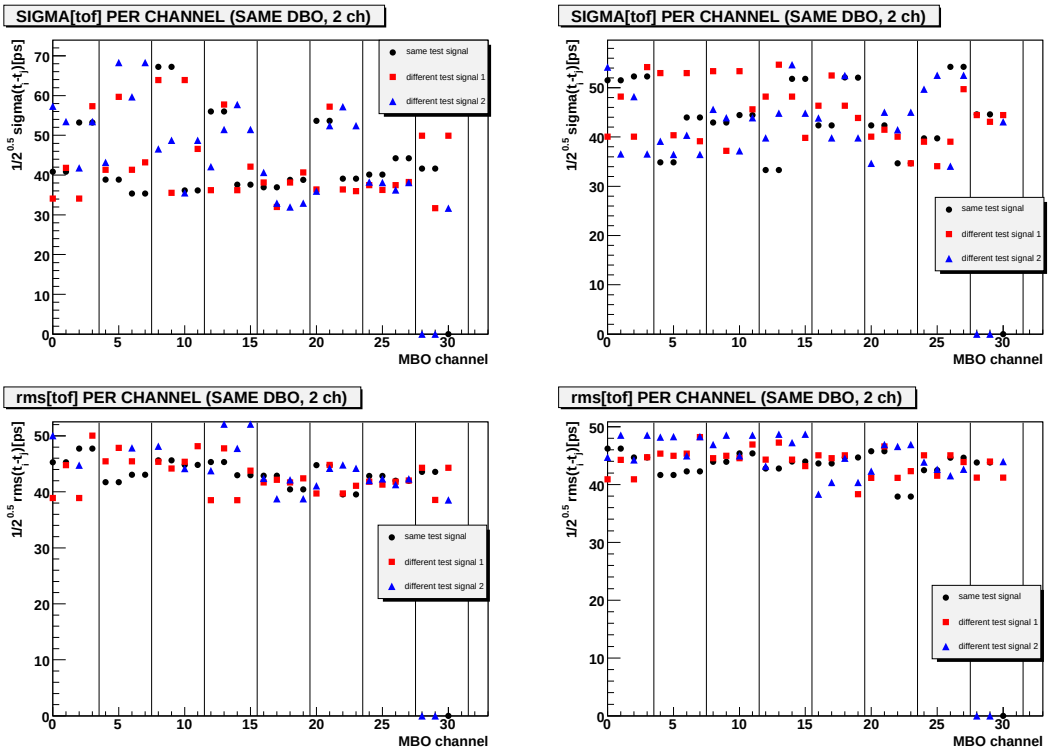


Figure 8.19: *Up: Time resolution σ_T for all the combinations of one MBO with an environment temperature, ∼25 °C, (left) and 70 °C (right). Down: the same for the rms_T, both measured with test signals.*

environment temperature changes between 30 and 70 ps per channel and for T=70 °C is even better, changing between 30 and 60 ps per channel (this improvement is not significant). The rms_T has also the same behaviour for both temperatures, changing between 40 and 50 ps for all the combinations of each MBO.

Measurements of the width of the LVDS signal (QtoW) and its jitter were also done, verifying that the behaviour was the same when we reached values of T=75 °C.

8.6.2 Assembly of all the RPC sectors

As was mentioned before, the assembly of the six RPC sectors was done in groups of two and, finally, all of them were installed in the HADES spectrometer. Each pair of RPC boxes were validated with a cosmic rays test, being developed at GSI.

Before the cosmic ray test, each sector was assembled with the corresponding final version of the FEE [56], [57]: 12 MBOs, 4 miniMBOs and 108 DBOs. The FEE was fed by two low voltage boards [108] for each sector, taking into account the power consumption levels required for the final version of the FEE shown in Table 8.2: one channel (∼0.5 W), one DBO, one MBO, one full RPC sector and all the six sectors. The DAQ system consists of five TRBv2 [86] per sector.

	1 DBO	1 MBO	1 FEE channel	1 RPC sector	6 RPC sectors
Power consumption	1.97 W	1.55 W	0.5 W	233.8 W	1.4 kW

Table 8.2: *Power consumption of the final version of the FEE, showing the values of individual channels, DBOs, MBOs, one full sector and the full six sectors, respectively.*

Figure 8.20: *Experimental setup of the HADES RPC wall commissioning, showing four assembled sectors with the FEE boards (left) and two stacks of five TRBs each for the DAQ system (right).*

Figure 8.20 shows the experimental setup implemented at the cosmic rays tests developed during the RPC commissioning. As is shown in the left picture, two RPC sectors were assembled one above the other, to have the choice of triggering in coincidence in both sectors (events which give a signal in both sectors). The trigger signals coming from each MBO were summed in external 8-channel summing boards, being two of them needed for triggering in both layers of one side of both sectors. The DAQ system is based in the TRBv2 and two stacks with five boards each are required (see Fig. 8.20-right), four to acquire the full sector and other one to distribute the trigger signal. With external CAEN modules (a discriminator and a module of coincidences) we discriminated the trigger signal to select the multiplicity trigger signal needed in both sectors.

Some results are shown in Figures 8.21 and 8.22. The first plot presents the time resolution σ_T of all the cells corresponding to the sector 5, distributed in three rows in two layers. The mean value obtained for this sector is $< \sigma_T >$=76.61 ps/channel. The second picture shows a QtoW spectrum of one cell obtained with cosmic rays, showing the streamers region, clearly separated of the normal avalanches region. The minimum value of the QtoW spectrum is ∼55 ns, corresponding to signals without charge, and the maximum is ∼400 ns, corresponding to streamers.

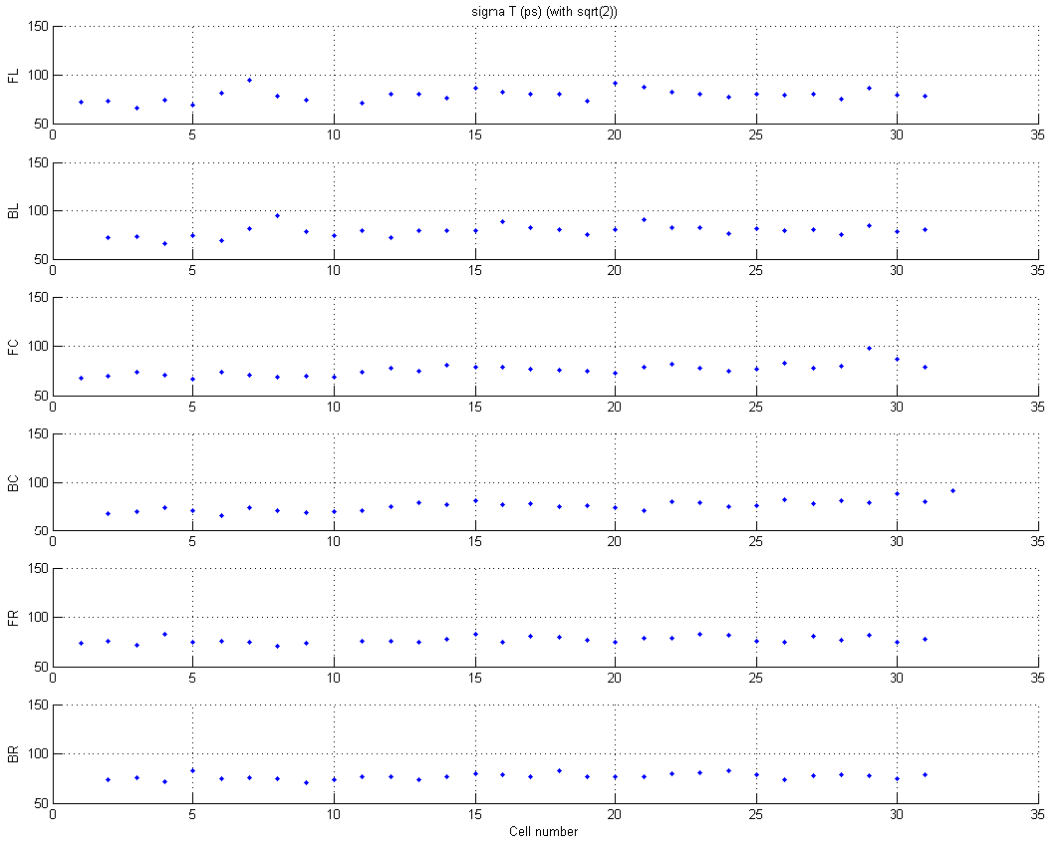


Figure 8.21: *Time resolution σ_T of all the cells of the sector 5, showing a mean value of 76.61 ps/channel, measured with cosmic rays.*

8.6.3 Installation of the RPC sectors in HADES

The installation of the whole six RPC sectors, including the FEE and the data acquisition system, in their nominal positions inside the HADES spectrometer was done at the end of 2009, between November and December (see pictures of Fig 3.13). With this installation the upgrade of the HADES ToF wall with the RPC detectors is finished and the spectrometer is ready to take data along 2010.

8.7 HADES RPC ToF wall conclusions

With the commissioning and the installation of all the sectors and their correct performances regarding stability of the system, time resolution, charge information, crosstalk and efficiency [69], [56], [107], the construction of the timing RPC detectors, the FEE assembly and the final installation in the HADES spectrometer is finished. And we finished with more than five years of work, mainly an international collaboration between the LIP in Coimbra (Portugal), the USC-LabCAF in

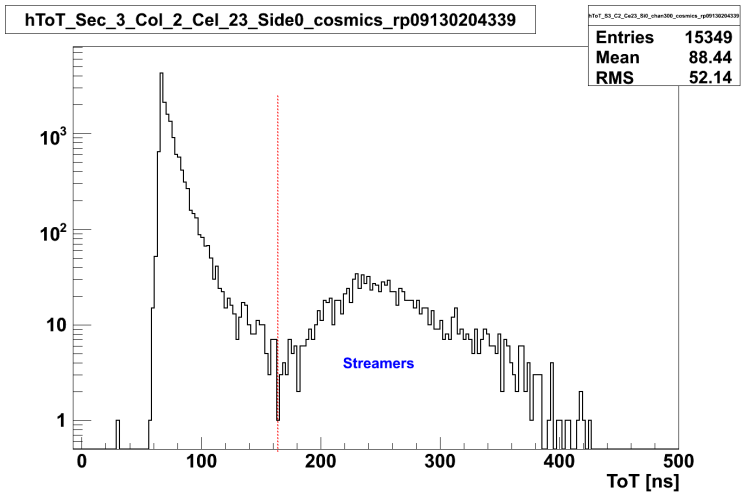


Figure 8.22: *QtoW spectrum of one side of a cell measured with cosmic rays, clearly separated the streamers and the normal avalanches regions.*

Santiago de Compostela (Spain), the GSI in Darmstadt (Germany) and the IFIC in Valencia (Spain).

But with the installation, the work is not finished yet. Along 2010, the HADES spectrometer is ready to take beam-time data and next years more experiments will be developed inside FAIR at GSI. So, more people will continue this work and analyze new data.

Chapter 9

Conclusions and Outlook

Each one of the chapters included in this thesis has its own conclusions. Therefore, we summarize in the next paragraphs the most important achievements related with the Front-End Electronics we have designed, developed, tested and installed for the HADES tRPCs wall.

The Front-End Electronics presented satisfies the main features that were required when the project started, concerning time resolution, efficiency and stability. The final design consists of two different boards:

1. A 4-channel active DaughterBOard (DBO) housing the preamplifying and the digitizing stages, described widely in this work.

2. A 32-channel passive MotherBOard (MBO) providing the regulated voltage, the test signals, the threshold levels and the final summing stage of the output trigger signal. The convenience of this second board was a consequence of the present work, and its final design was diverted to the IFIC of Valencia.

The FEE boards are powered by a low voltage board, based on switching DC-DC converter modules, which are prepared for voltage and current monitoring. The MBO delivers all LVDS signals to a Time-to-digital converter Readout Board (TRB), which is the main component of the DAQ system.

We have concentrated our effort in the design and testing of the DBOs, together with the installation and commissioning of the whole electronics in the six RPC sextants needed to cover all the low angle region of the HADES spectrometer.

The final version of the DBO uses a fast 1-2 GHz amplifier feeding a fixed threshold discriminator. Both time and charge information are encoded in the leading edge and in the width, using a 'Charge to Width' (QtoW) algorithm, of an LVDS digital output signal. Every eight DBOs are housed in a MBO getting from them stable and low ripple power supply voltage and ground, programmable thresholds controlled via DACs, test signals and paths for the readout of all the detector and trigger signals.

Main performances of the FEE are summarized in the next table.

Power consumption	Noise level	Crosstalk	Time resolution	QtoW range	Charge resolution	Physical threshold
<0.5 W/ch	<100 μV_{RMS}	<1%	16±5	<4 pC	<10%-σ	30 fC

Table 9.1: *Main features of the FEE final version, all of them for a single channel: power consumption, noise level, crosstalk, time resolution, QtoW range, charge resolution and the physical threshold.*

These performances are the following:

- Power consumption of <0.5 W/channel, being ∼1.4 kW for all RPC sectors.
- The noise level was minimized at the level of 5 mV at the output of the preamplifier (<100 μV_{RMS} at the input), indicating the minimum threshold level for avoiding the noise.
- There are no crosstalk effects for thresholds above 3 mV, being <1% below this value.
- The FEE time resolution was measured at the level of σ_T=16±5 ps/channel, being <40±5 ps/channel including the TRB board. The mean value of the time resolution of the whole chain, including the RPC detector, is σ_T=76 ps per channel, exhibiting modest timing tails at a level of 2% for 3σ tails.
- The mean value of the jitter of the QtoW algorithm is Δt=150 ps/channel, providing a charge resolution below 10%-σ for avalanche pulses with q_p>50 fC. The QtoW range is linear for signals q_p<4 pC, extending the range until charges at the level of 25 pC but with the amplifier saturated in amplitude. The QtoW algorithm clearly separated normal avalanches from streamers.
- The physical threshold of the FEE is at the level of ∼1 mV, corresponding to a charge of ∼30 fC at the input of the preamplifier.

Final DBOs boards have been reduced to a compact (4.5×5 cm^2 for four channels) and very stable design.

In the last months of 2009, all the HADES tRPC sectors have been instrumented and tested successfully, being ready now for the first run of experiments, scheduled for spring 2010.

Appendix A

FEE-STEP1 and STEP2: schematics and layouts

This appendix is focused to explain the schematics and the layouts of the two first FEE designs developed for the HADES RPC wall, the so-called FEE-STEP1 and FEE-STEP2. Both designs were developed with the ORCADv9.1 [81].

A.1 FEE-STEP1 schematics and layout

Figure A.1 shows the layout of the STEP1 [39]. The board dimensions are 10.5×3 cm^2 (∼31 cm^2). It houses one channel per board, with two layers (TOP is the blue layer and BOTTOM the red one). All the components are distributed in both layers, although most of them are in the TOP layer.

Figure A.2 shows the schematic of this board in detail, with all the components explained in chapter 3: the active components (preamplifiers, discriminator, delay line...) and the passive ones (resistors, capacitors and inductances).

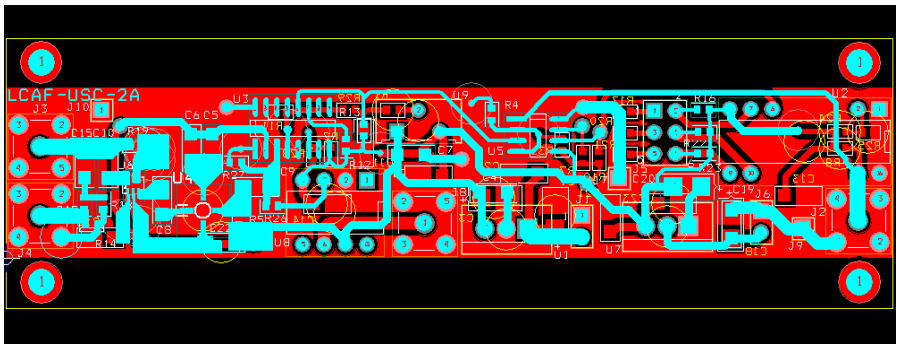


Figure A.1: *One-channel layout of the FEE-STEP1 board with two layers: TOP layer (blue) and BOTTOM one (red). The size is 10.5×3 cm^2 (∼31 cm^2).*

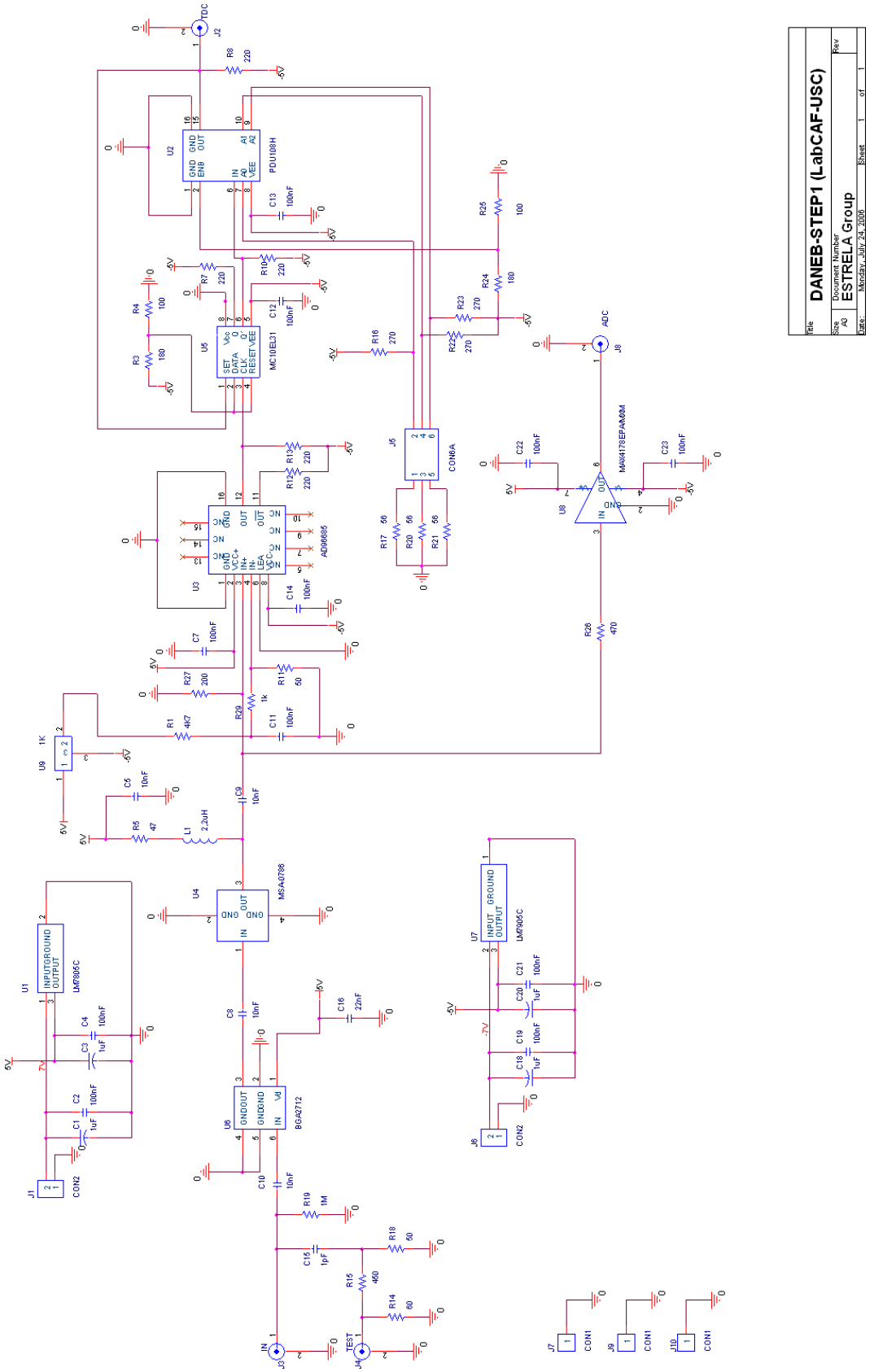


Figure A.2: *Schematic of the FEE-STEP1 board, showing the analog (lower part) and the digital stages (upper one) corresponding to one channel.*

A.2 FEE-STEP2 schematics and layout

Figure A.3 shows the layout of the STEP2. This trapezoidal shape was chosen to fit the free available room between different timing RPC sectors in HADES. The STEP2 design [39], [79] is a 2-channel 4-layer board (TOP and BOTTOM for distributing components and two internal layers for the ground and power supply planes). The dimensions of the STEP2 board were $\sim 6 \times 4$ cm^2, corresponding to ~ 24 cm^2. In this FEE-STEP2 design, the critical dimension for geometric detector reasons was the 4 cm width in order to avoid that PCBs of the several sectors crash between them, as it was explained in chapter 3 (see section 3.6 and the right picture of Fig. 3.10).

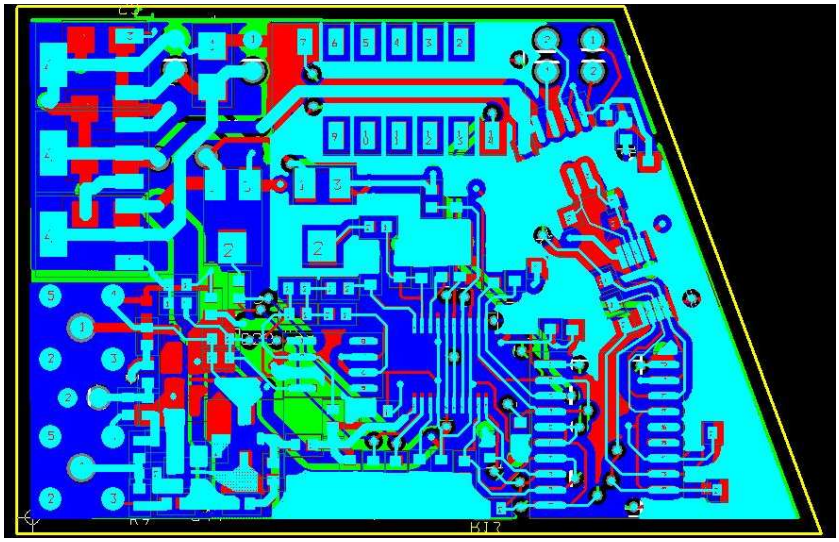


Figure A.3: *Layout of the FEE-STEP2 board, showing two channels per board in the TOP layer (blue) and the BOTTOM one (red). Also the two inner layers for grounding and power supply planes are shown.*

Figures A.4 and A.5 show the schematic of the board in detail, with all the components for both channels. Figure A.4 shows the voltage regulation, the threshold level required for the discriminator and the analog stages (including both amplifier stages).

Figure A.5 shows the digital stage (with the final discriminator, the flip/flop, the delay line and the PECL to LVDS converter). Passive components (resistors, capacitors and inductances), with its exact values, are also shown. Both figures show the schematics corresponding to both FEE channels.

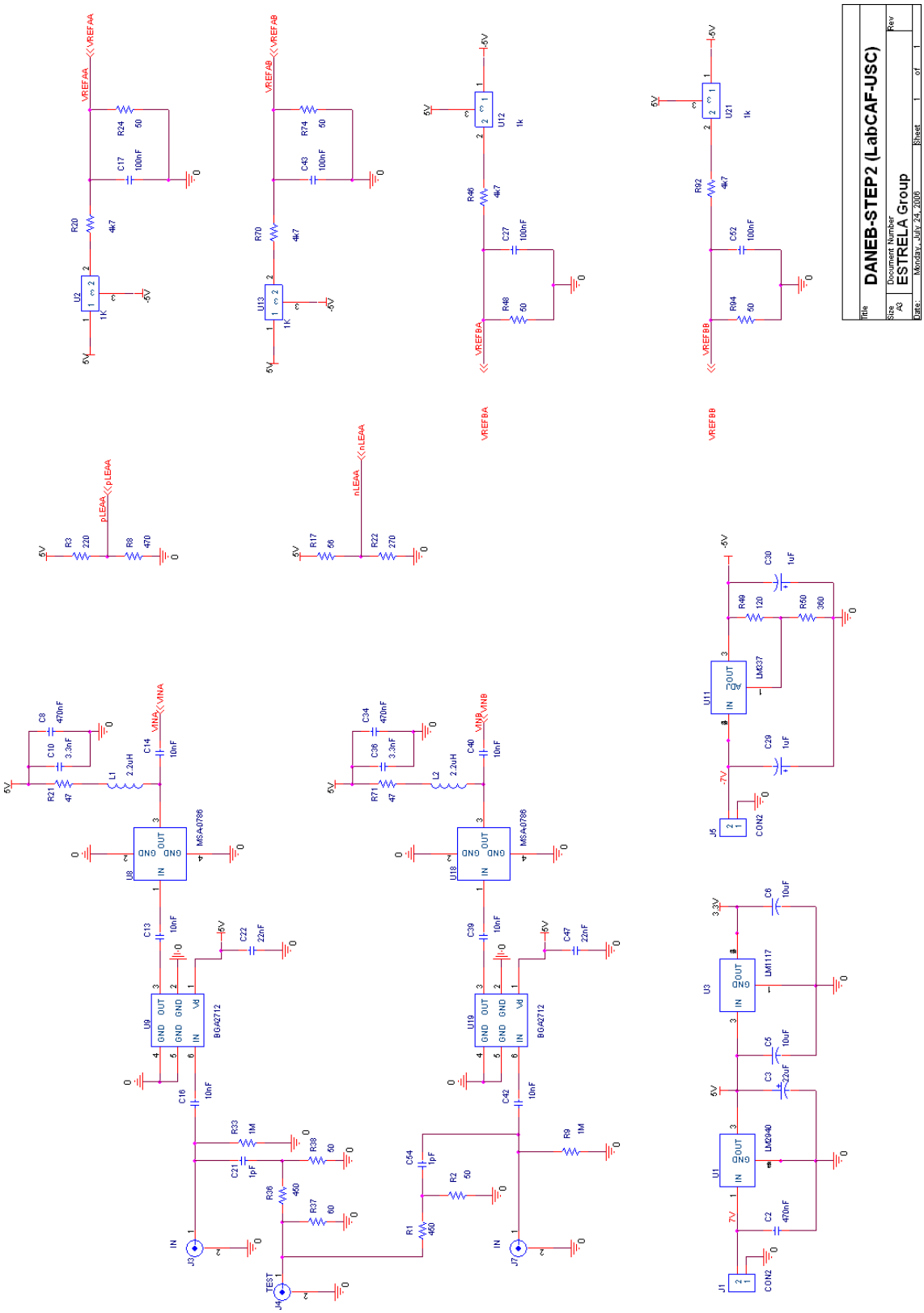


Figure A.4: *Schematics of the FEE-STEP2 board: two channels showing the voltage regulation and the analog stage, both in the lower part.*

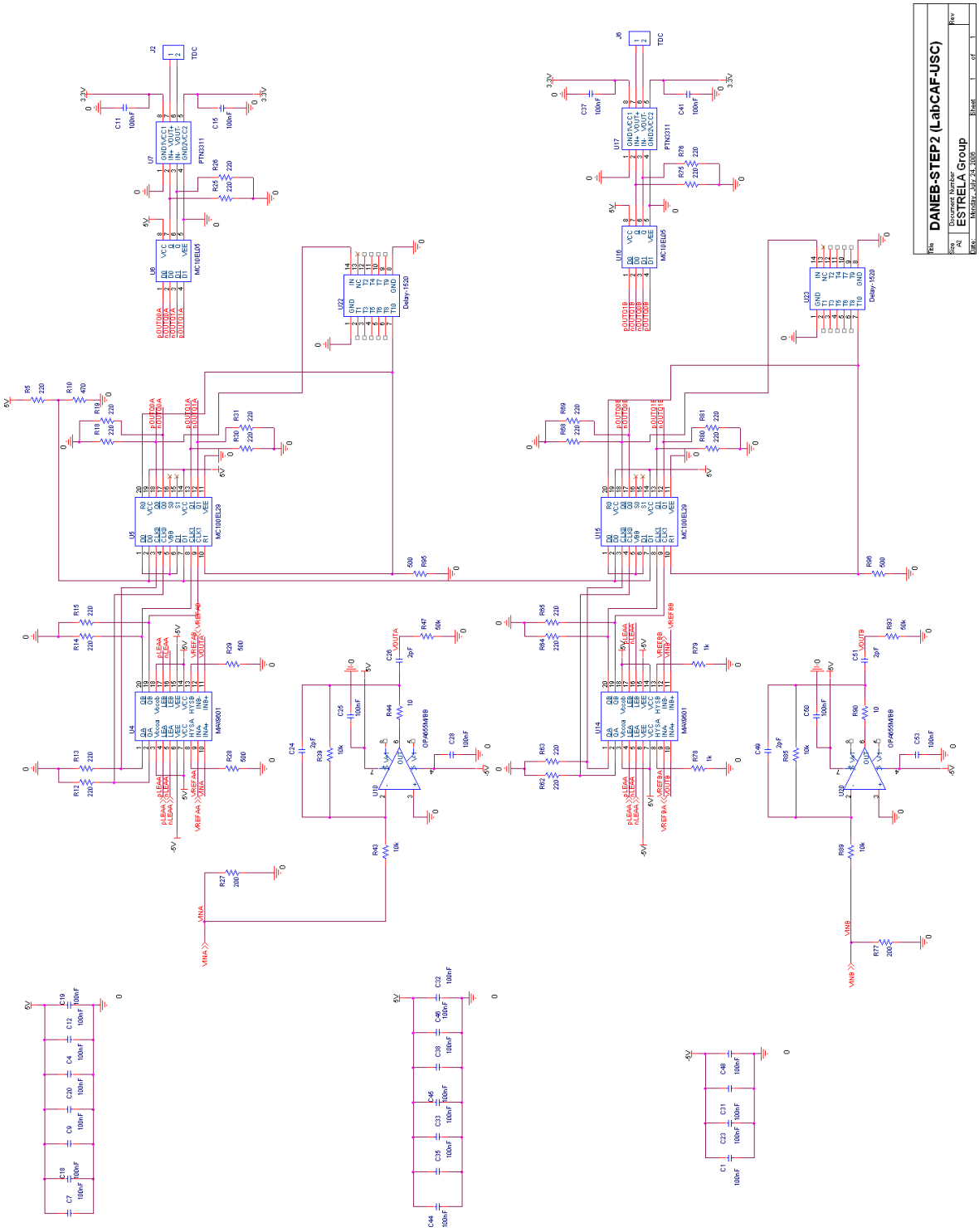


Figure A.5: *Schematics of the FEE-STEP2 board, corresponding to the digital stage of two channels.*

Appendix B

Different designs with DBO-MBO configuration

From FEE-STEP3 to STEP6 final board, we used a MotherBOard-DaughterBOard (MBO+DBO) configuration. This appendix presents the schematics and the layouts of the some of these FEE designs corresponding to the HADES timing RPC wall, including the MBOv2, similar to the final version of the MBO (only small changes were implemented). The development of all designs was done with ORCADv9.1 [81] and EAGLEv4.11 software.

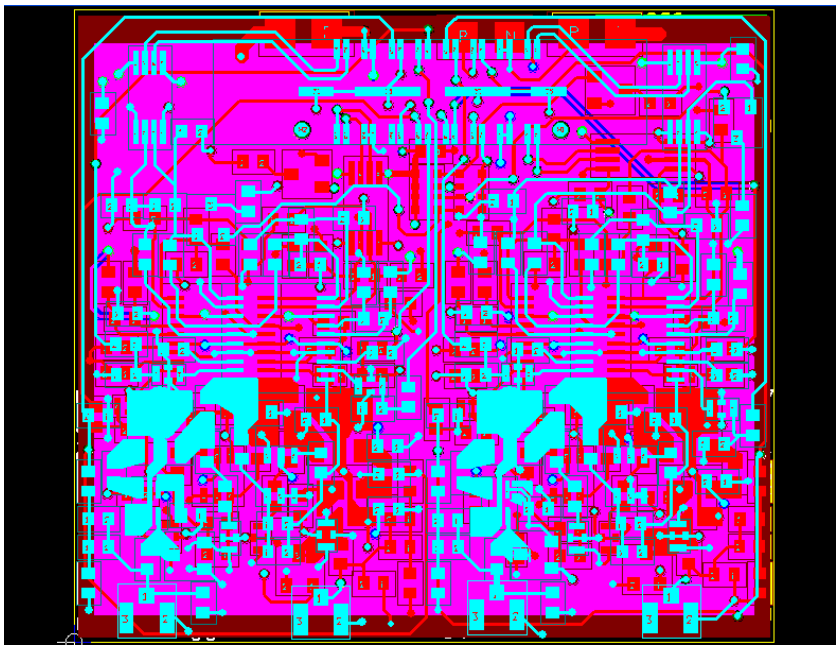


Figure B.1: *Layout of the DBO-STEP3, showing the four channels of each board: two in the TOP layer (blue) and two in the BOTTOM one (red). The size is 5×4.5=22.5 cm^2.*

B.1 DBO-STEP3 schematics and layout

Figure B.1 shows the layout of the DBO-STEP3 board. The board dimensions are 5×4.5=22.5 cm^2. The DBO-STEP3 design [80] is a 4-channel board, with 6-layers (TOP is the blue layer and BOTTOM the red one and the other four layers are inner layers for ground and power supply planes). All the components are placed in the TOP and BOTTOM layers, two channels in each layer.

Figures B.2 and B.3 show, respectively, the schematics of the analog and the digital stages of this board in detail with all the components: the active components (preamplifiers, discriminator, converter, transistor..) and the passive ones (resistors, capacitors and inductances).

The schematics and the layout of the DBO-STEP4 design are similar to the ones of the previous STEP3: the only differences between them are that the STEP4 design has only one preamplifier (the GALI-S66, the second preamplifier of the STEP3) and the PTN3311 PECL/LVDS converter was changed by the SN65LVDT100 model.

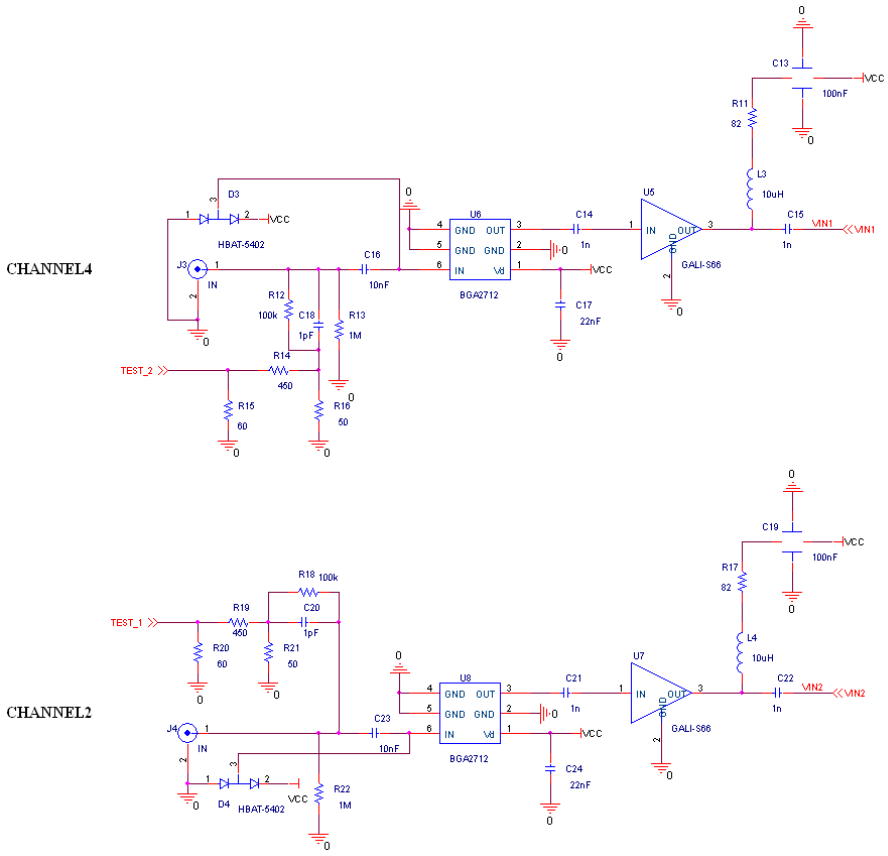


Figure B.2: *DBO-STEP3 schematic, corresponding to the analog stage of two channels, showing both amplifier steps and the test input.*

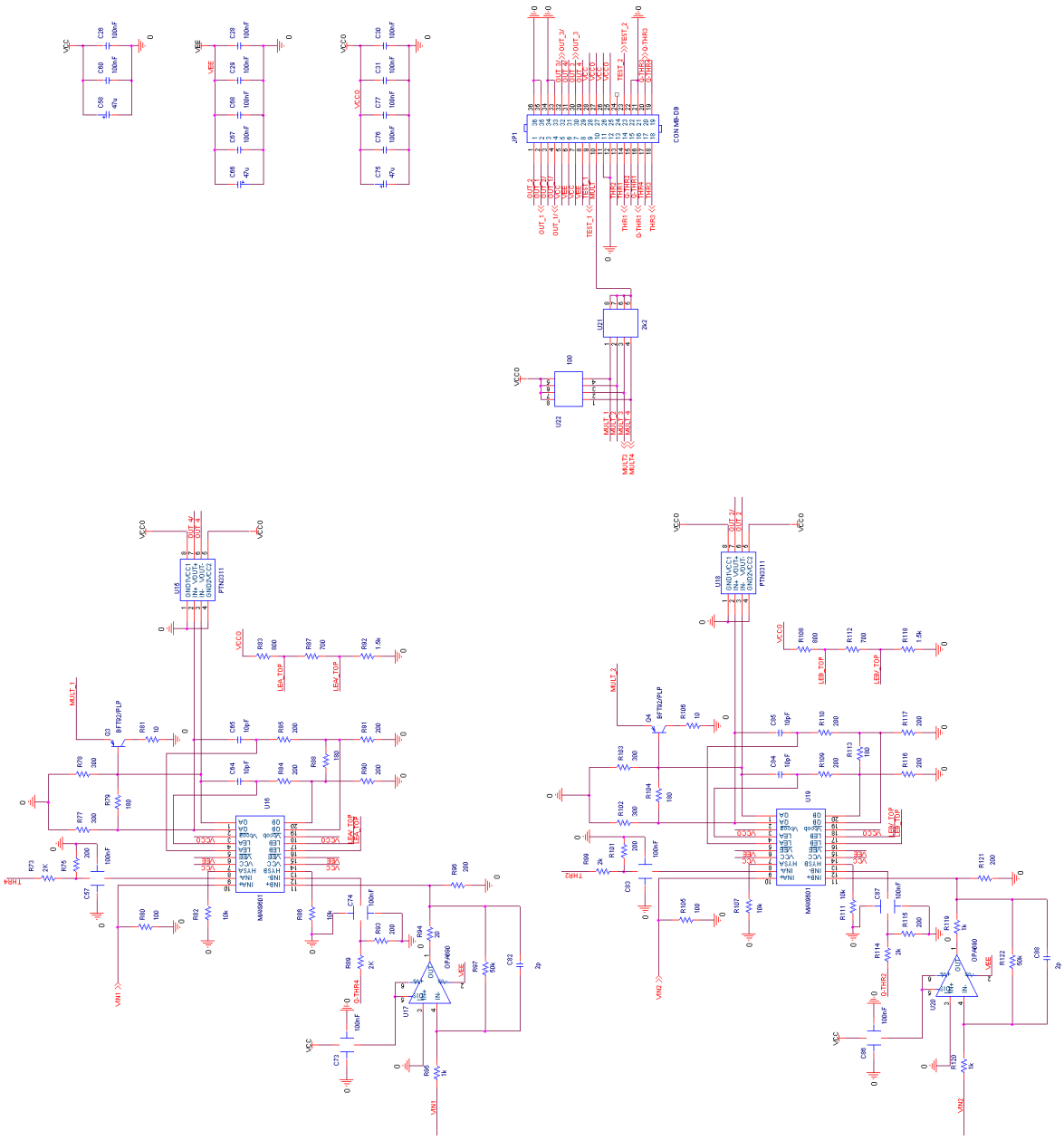


Figure B.3: *DBO-STEP3 schematic, corresponding to the digital section of two channels (of a total of four in each board), showing the integration, the discriminator and the converter steps.*

B.2 DBO-STEP5: schematics and layout

Two boards were developed of this design, being first the one at the University of Santiago de Compostela (USC) and after this the one at the GSI (Darmstadt, Ger-

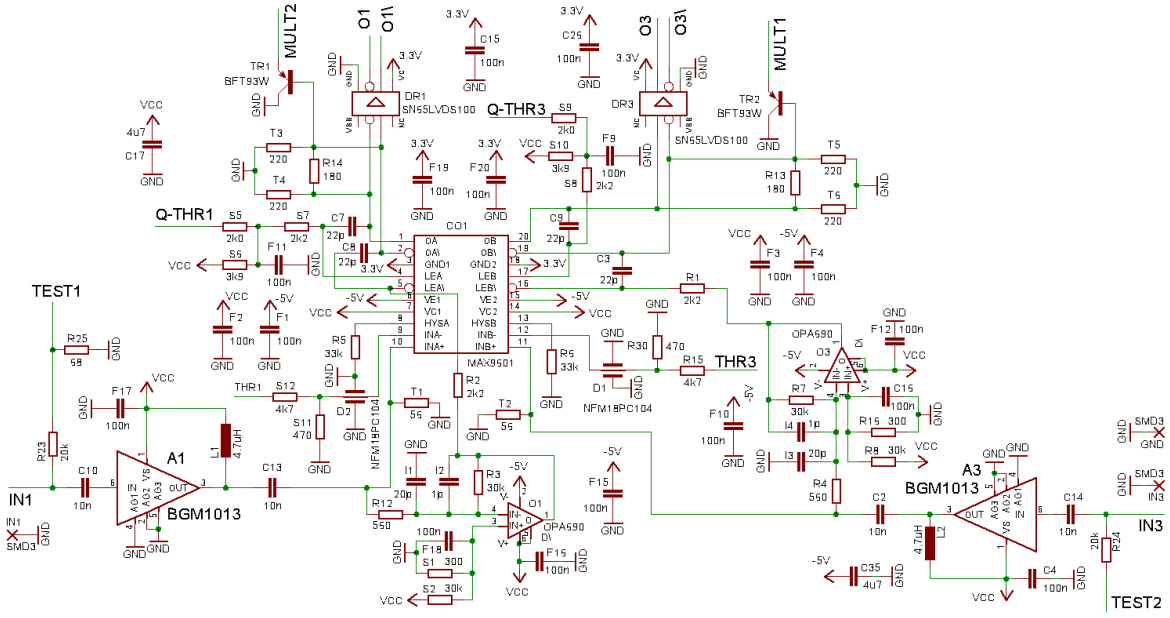
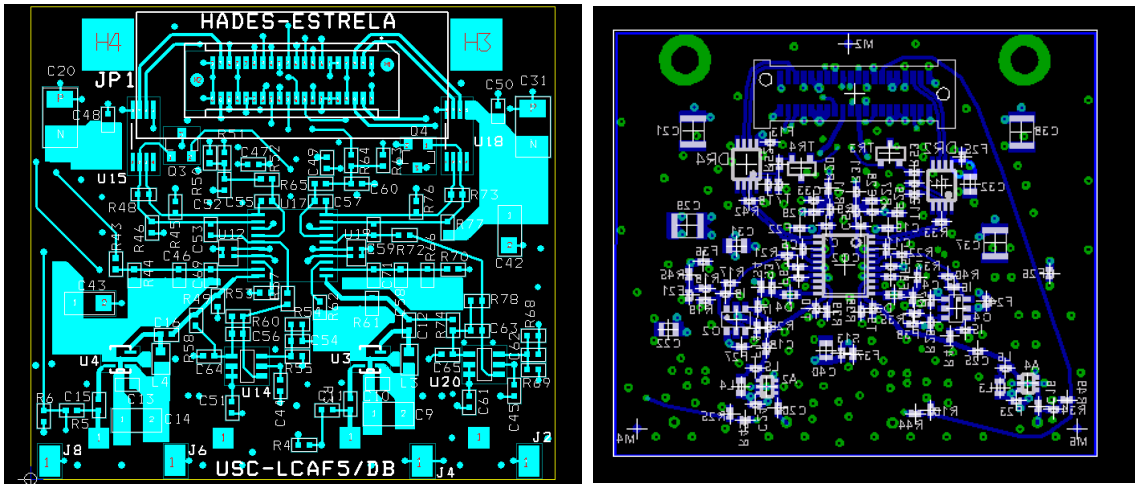


Figure B.4: *DBO-STEP5 schematic, corresponding to two channels of a total number of four, showing both analog and digital steps.*



(a) (b)

Figure B.5: *DBO-STEP5 layouts corresponding to the design developed in the USC (a) and in the GSI (b), showing the TOP layer in both cases. Its size is 5×4.5=22.5 cm^2, the same than previous version.*

many). The schematic of both boards is the same, being the small differences related with the layout. Figure B.4 shows the schematic of this board in detail, with all the components: the active components (preamplifiers, discriminator, converter...) and the passive ones (resistors, capacitors and inductances).

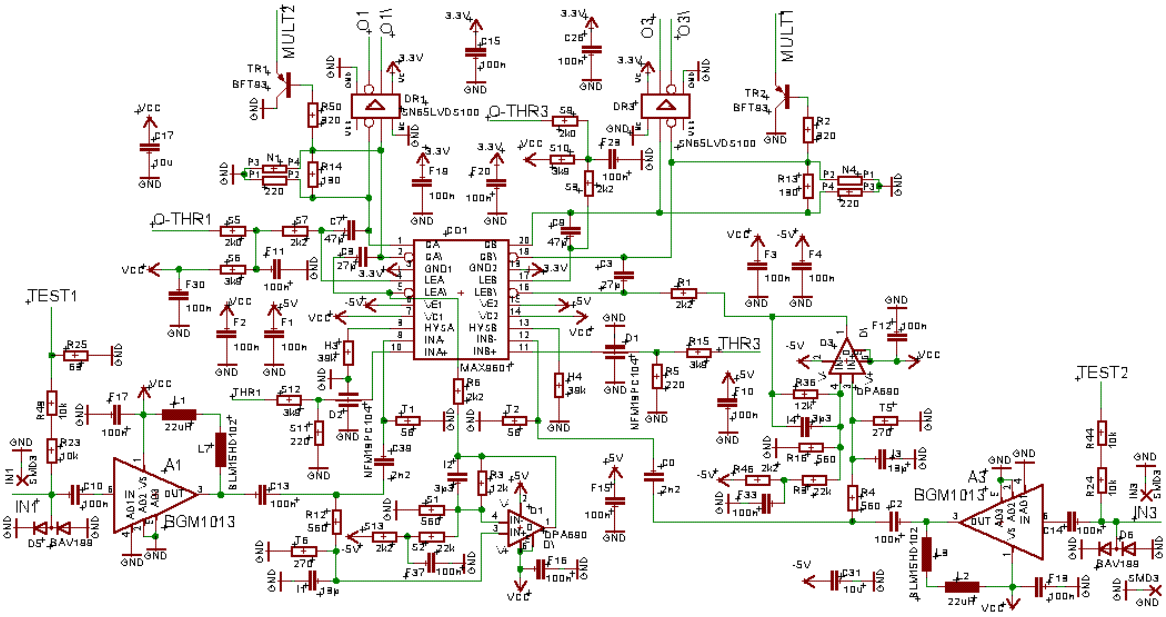


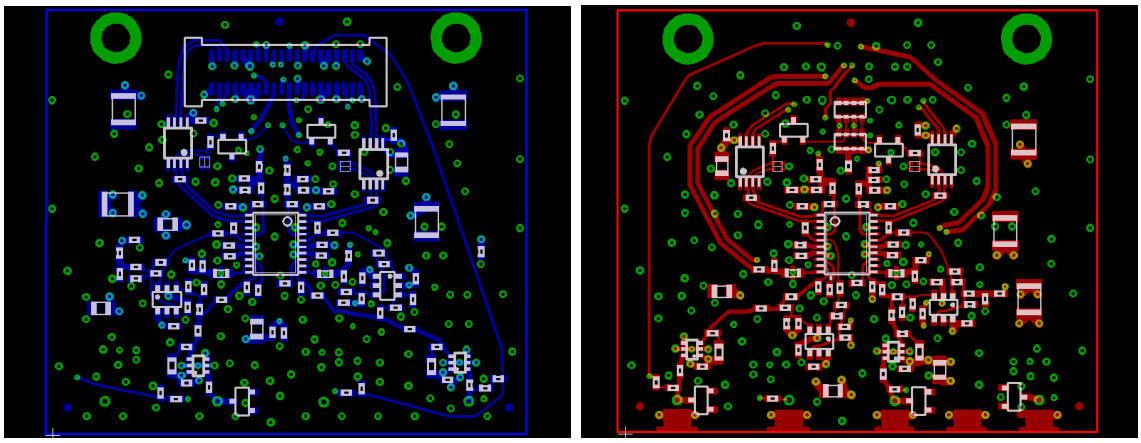
Figure B.6: *Schematic of the final version of the DBO, corresponding to two channels, showing both analog and digital steps.*

Figure B.5 shows the layout of the STEP5 of both boards. The board dimensions are 5×4.5 cm^2=22.5 cm^2, the same than the previous STEP3 and STEP4 designs. The STEP5 design [56] is a 4-channel board, with 6-layers (TOP is the blue layer in both pictures). All the components are placed in the TOP and BOTTOM layers, two channels in each layer. The remaining four inner layers are for routing, grounding and power supply planes.

B.3 DBO final version: schematics and layout

Figure B.6 shows the schematic of the DBO-STEP6 in detail, with all the components: the active components (preamplifiers, discriminator, converter...) and the passive ones (resistors, capacitors and inductances). The main differences respect DBO-STEP5 design is the negative signals expected at the output of the amplifier (a negative ToF thresholds are needed for the final version, provided by the MBO final design) and the asymmetry of the LE configuration instead of the symmetric configuration in the STEP5.

Figure B.7 shows the layout. The board dimensions are the same of the previous STEP5 board. The STEP5 design [56] is a 4-channel board, with 6-layers (TOP is the blue layer in both pictures). All the components are placed in the TOP and BOTTOM layers, two channels in each one.



(a) (b)

Figure B.7: *Layout of the final version of the DBO developed in the GSI, showing the TOP layer (a) and the BOTTOM one (b). Its size is 5×4.5=22.5 cm^2.*

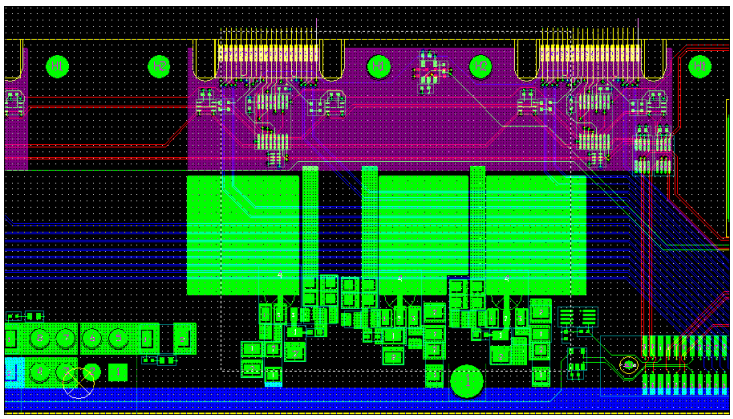


Figure B.8: *A detail of the MBOv2 layout, showing the -5 V power supply plane (violet area) over two main DBO block areas.*

B.4 MBOv2: schematics and layout

The MBOv2 has eight layers and all the components are placed in the TOP and the BOTTOM layers. The other ones are used for routing, grounding and power supplies planes. Adding the regulators complicated the layout because of the need of separated plane areas for the different voltages provided from the different regulators. For example, the violet area in Fig. B.8 represents the -5 V regulated power supply plane. The +5 V and +3.3 V planes are located at the same place but in different layers.

Figures B.9 and B.10 show the schematics of the MBOv2 [88], [89], housing the DACs for all eight DBOs, the test signals distribution, the trigger summing stage at the MBO level, the power supplies for all voltages and the connectors MBO-DBO

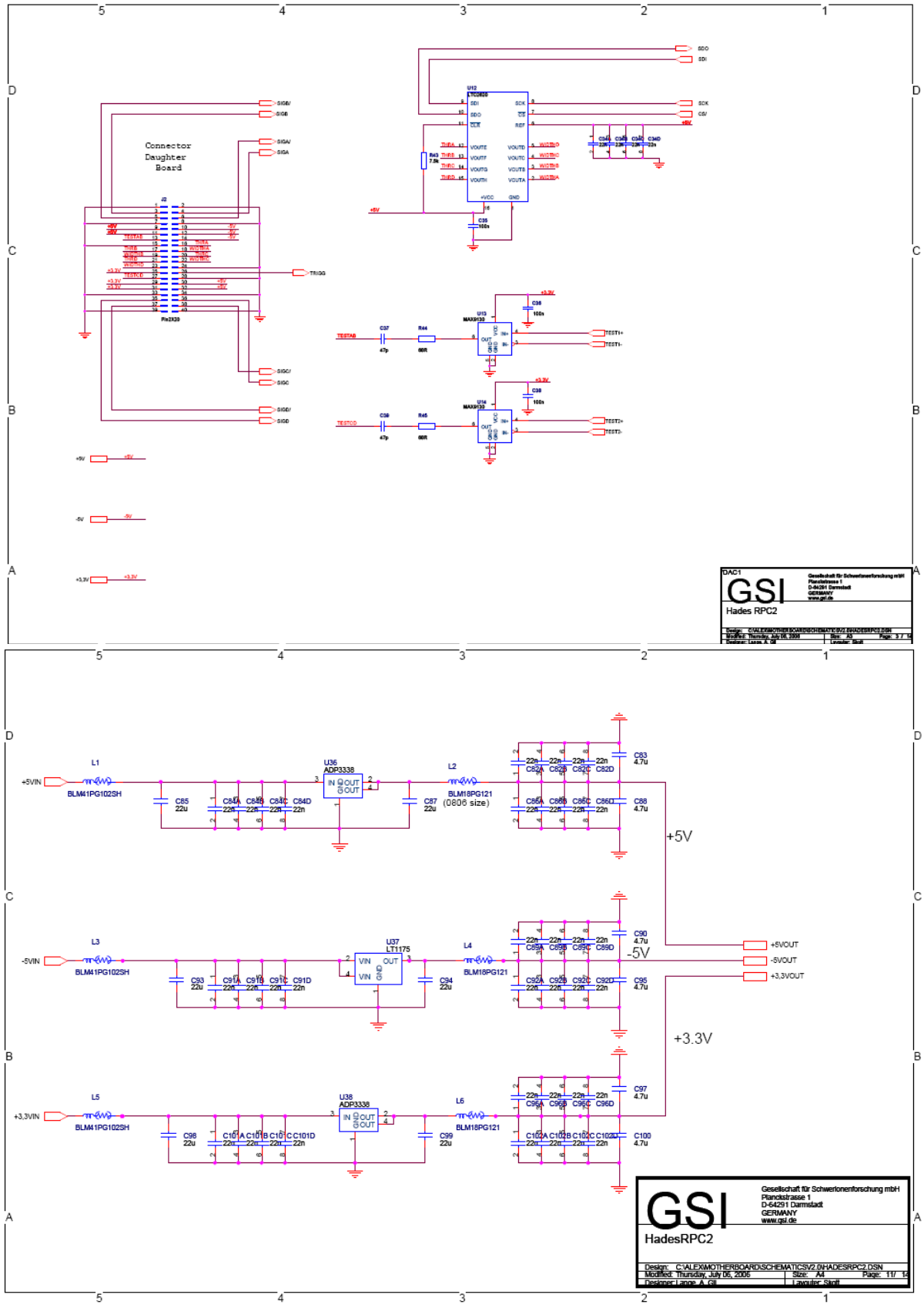


Figure B.9: *MBOv2 schematics, showing the threshold levels, the test signals and the MBO-DBO connector (up) and the voltage supply part (down).*

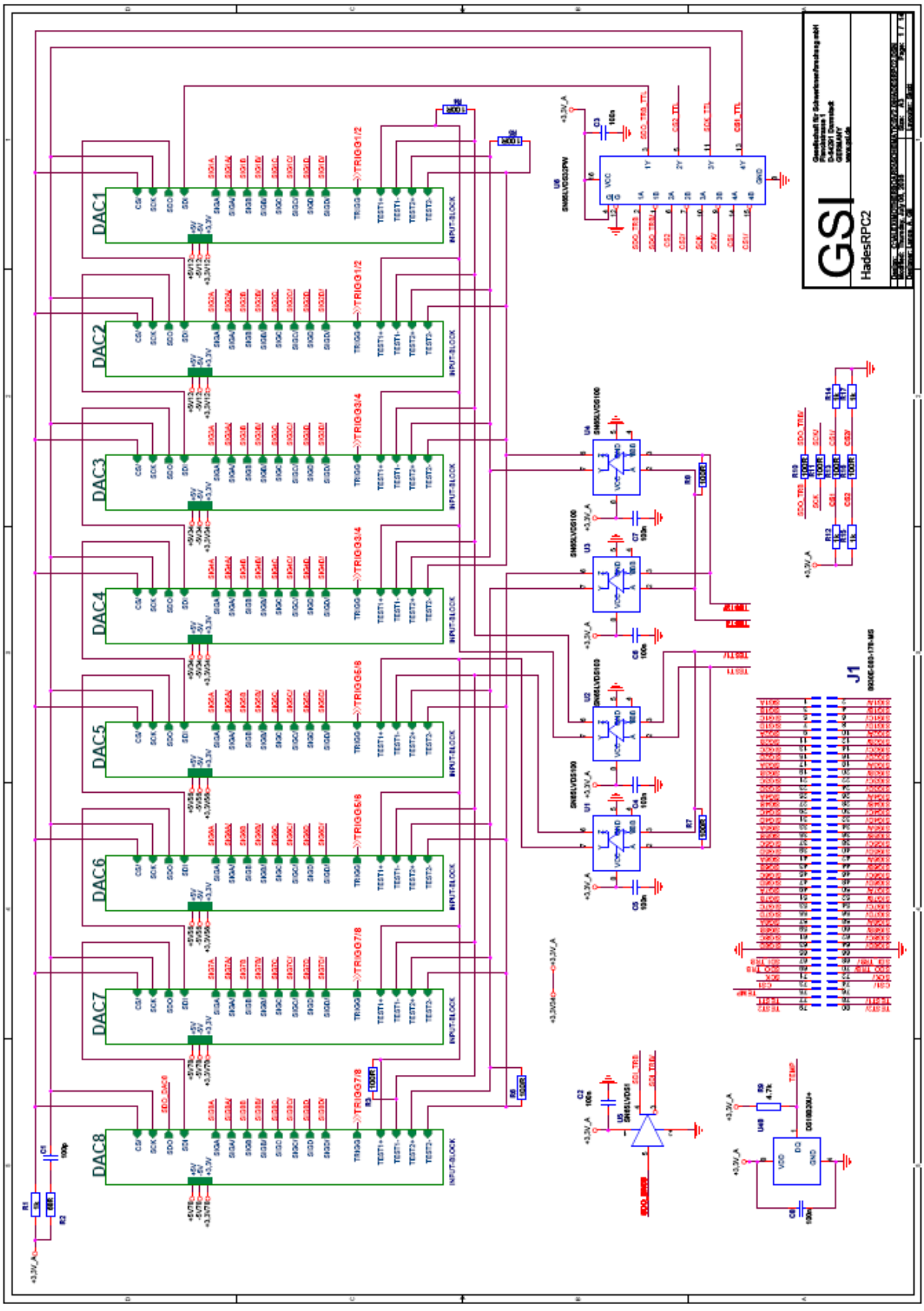


Figure B.10: *MBOv2 schematics, housing up 32 channels in each board divided in eight DBOs, showing the DAC stage (left) and the MBO-TRB connector (right).*

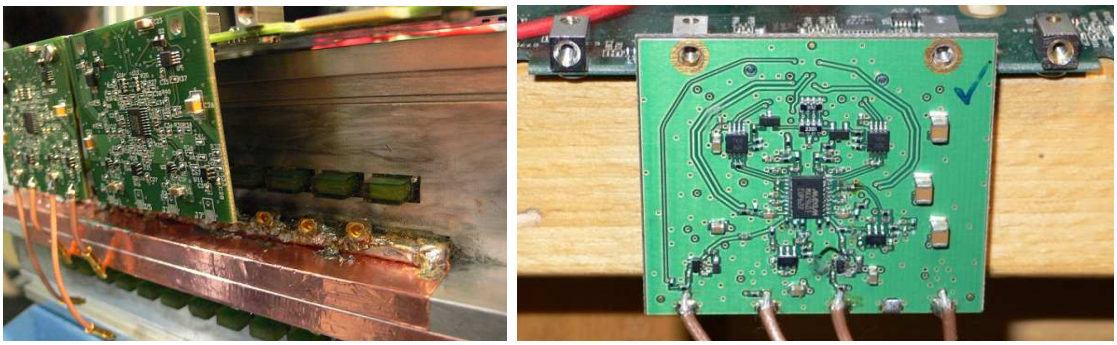


Figure B.11: *Two details for the MBOv2 and DBO-STEP5 connection.*

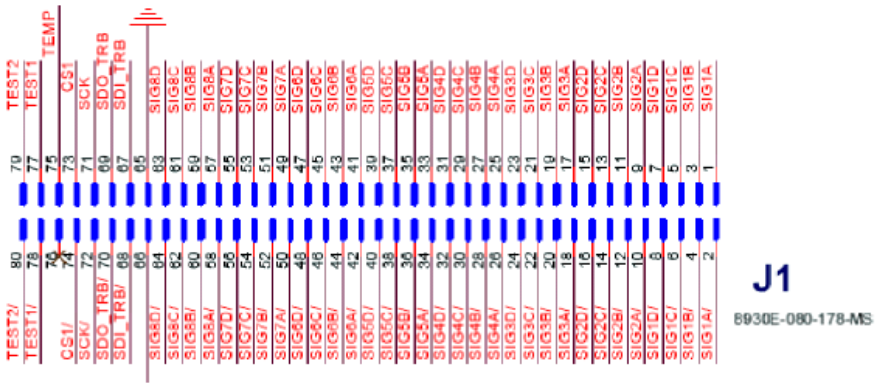


Figure B.12: *Pin-out assignment of the MBOv2 and TRB connector. The connector is the same than in previous version.*

and MBO-TRB. The dimensions of the MBOv2 are the same than the MBOv1, 40×6 cm^2=240 cm^2, allocating up to eight DBOs and 32 electronic channels. The schematics and layout are almost the same than the final version of the MBO.

Figure B.11 shows two details for the MBOv2 and the DBO-STEP5 connection. The left picture presents the connection between the FEE (DBO+MBO) and the RPC detectors and the right one shows the connection between MBO and DBO from the DBO side (showing one of the MBO blocks for each DBO).

Figure B.12 shows the pin-out assignment of the MBO-TRB connector, which is the same KEL8930 series with 80 pins used between the MBOv1 and the TRBv1. It shows both channel outputs (normal and complementary), the test signals and the line for the temperature sensor.

Finally, we show the schematic of the miniMBO (Fig. B.13) and two pictures of the miniMBOv1 and miniMBOv2 developed by the LabCAF group (Fig. B.14). These boards were designed only for testing the DBOs before the MBOs were finished. The schematic is the same for both designs, providing to the DBOs the three voltage power supplies (+5 V, -5 V and +3.3 V) via voltage regulators, the threshold

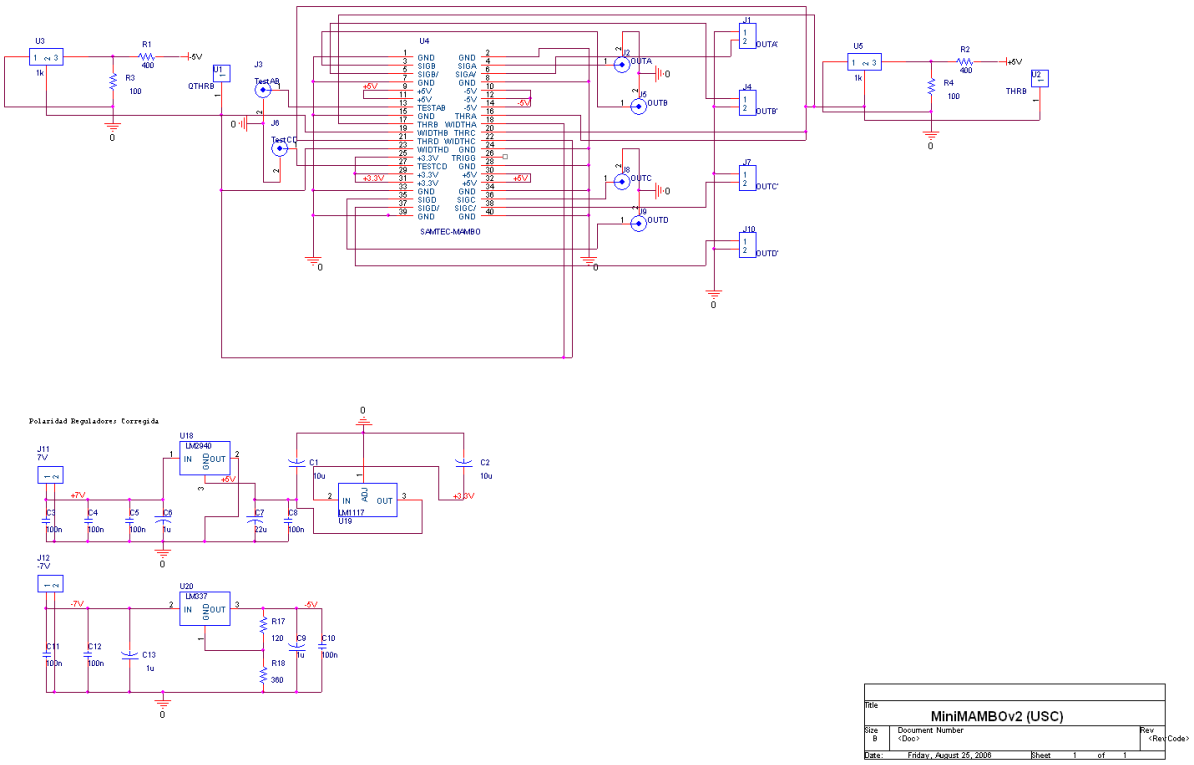


Figure B.13: *Schematics of the miniMBOv2 developed at LabCAF-USC.*

Figure B.14: *Pictures of miniMBOv1 (left) and miniMBOv2 (right).*

levels for the ToF and the ToT discriminators, both through potentiometers which provided the range needed, and the test inputs needed to inject external pulses.

Appendix C

Resumo

C.1 Introducción

O traballo que se presenta nesta tese forma parte do proxecto que pretende cubrir, cun muro de detectores RPCs de tempo de voo, a rexión de ángulos baixos do espectrómetro HADES[1], que se encontra no centro de investigación GSI en Darmstadt, Alemaña. HADES foi concebido para estudiar materia nuclear densa a través de pares de di-leptóns procedentes do decaemento de mesóns vectoriais lixeiros. Como parte deste proxecto, un muro de RPCs (placas paralelas resistivas) de tempo de voo ou 'timing RPCs' (tRPCs) construíuse como mellora do espectrómetro orixinal, permitindo estudar colisións de ións pesados ata Au+Au a enerxías cinéticas da orde de 1.5 GeV/A.

O muro de tempo de voo está basado en RPCs, que tiveron a súa orixe nos anos 80 co primeiro prototipo desenvolvido por Santonico [21], con resolucións temporais ó nivel de 1 ns. A observación, no ano 2000, da gran importancia da constancia da distancia da separación entre electrodos, permitiu mellorar as resolucións temporais ó nivel de 50 ps, dando lugar a que as RPCs sexan competitivas cos centelladores máis rápidos e tendo ademáis a grande vantaxe de proporcionar un precio por canle moito menor. Co desenvolvemento destas RPCs de tempo de voo, que acadan resolucións temporais inferiores a 100 ps, ábrese a posibilidade de aplicación en diversos experimentos de Física de Partículas a enerxías altas e intermedias.

Tendo en conta as características do espectrómetro HADES, o deseño do muro de tRPCs debe cumprir os seguintes requisitos [22], [69]:

- Cubrir unha área de $\sim$8 m^2, dividida en seis sectores diferentes.
- Nivel de ocupación por celda por debaixo de 20%, recomendado por debaixo do 10% para a detección de leptóns, e alta granularidade.
- Alta capacidade multi-traza para taxas cercanas a 1 kHz/cm^2.

[1] High Acceptance Di-Electron Spectrometer

Figure C.1: *Celdas para a montaxe do muro de RPCs do espectrómetro HADES (ver capítulo 3).*

- Unha resolución temporal homoxénea por debaixo de 100 ps, cunha presencia moderada de colas e un nivel baixo de interferencia entre canais (*crosstalk*).
- Alta eficiencia intrínseca e xeométrica, cercana ó 100%.
- Necesidade dunha electrónica de amplificación e dixitalización compacta, robusta, rápida e con pouco nivel de ruído para adquirir moitos canais baixo condicións estables.

Dada a alta granularidade requerida polo detector, e co obxeto de minimizar o posible *crosstalk* entre celdas e proporcionar boas prestacións no caso de exisir trazas simultáneas en celdas próximas, decidiuse dende un principio empregar un deseño de celdas *multigap* ailladas electricamente. Para manter ó nivel de ocupación das celdas constante a niveles inferiores ó 20%, decidiuse segmenta-la área activa en 3 columnas, tendo celdas de anchuras diferentes nas distintas rexións de ángulos polares. Debido ós espacios mortos entre celdas, foi proposta unha xeometría en dúas capas (ver Fig. 3.10) e o solape é fixado de maneira que todas as trazas de interese atravesen, polo menos, 4 ocos de gas, garantindo eficiencias intrínsecas preto do 99% [38]. A estructura das celdas móstrase na Fig. D.1, correspondentes ós seis sectores definitivos. Cada celda ten 4 gaps de 0.3 mm de grosor

O último punto correspondente ós requisitos do muro de tRPCs sobre o deseño dunha electrónica de amplificación e dixitalización é a parte central do traballo desenvolvido nesta tese.

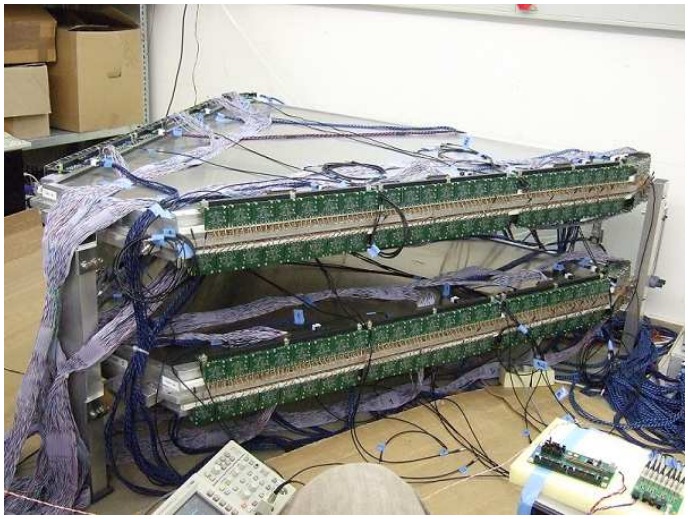


Figure C.2: *Versión final da electrónica de amplificación e dixitalización implementada en dous sectores de RPC, dividida en dúas tarxetas: DBO e MBO. A montaxe experimental corresponde ó 'commissioning' do proxecto.*

C.2 Electrónica de amplificación e dixitalización

O deseño da electrónica de adquisición do muro de RPCs do espectrómetro HADES ten que cumprir unha serie de requisitos [69]:

- Unha resolución temporal para medidas de tempo de voo <100 ps rms por canle. Debido ó rápido tempo de subida dos sinais do detector (∼300 ps), precisamos dun preamplificador cun gran ancho de banda (∼1-2 GHz).

- Información temporal e de carga precisa, codificadas nun único sinal dixital, reducindo así o número de canais de electrónica de adquisición. Os niveis do sinal dixital de saída deben ser compatibles co sistema de adquisición.

- Un deseño compacto, estable e co menor número de compoñentes (debido ó pouco espacio) para minimiza-lo ruido e o *crosstalk* e moderar o consumo.

- Conseguir unha eficiencia do detector superior ó 95% ás taxas altas esperadas en HADES ($\Phi \leq 700$ Hz/cm^2).

Para chegar a un deseño definitivo da electrónica desenvolvemos diferentes versións. A primeira versión, coñecida como STEP1, baseada nunha electrónica previa deseñada no LIP en Coimbra [78], consistía nunha tarxeta dun canle, con dúas etapas amplificadoras e unha saída dixital ECL e un consumo elevado (en 10.5×3 cm^2, ver Fig. 4.1). E a última versión consiste en dúas tarxetas, chamadas DaughterBOard (DBO) e MotherBOard (MBO) [56] (Fig. D.2).

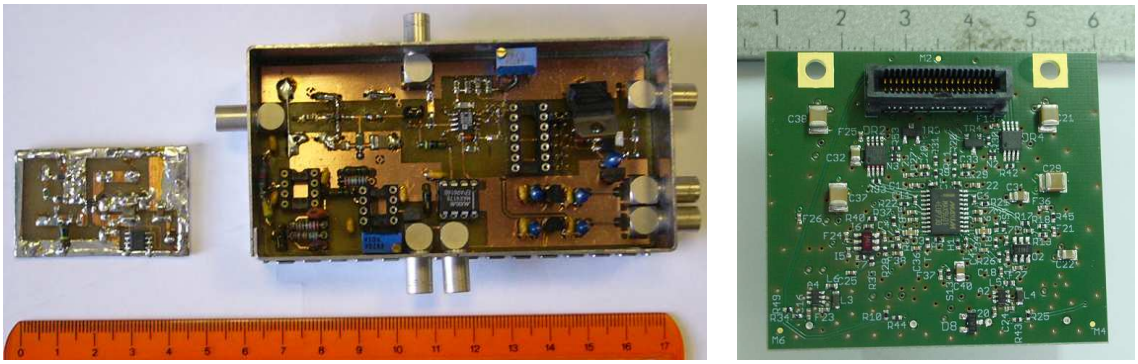


Figure C.3: *Adaptación da electrónica de referencia (left), desenrolada polo LIP en Coimbra [78] e formada por 2 tarxetas de preamplificación e dixitalización e versin final da DBO- STEP6 (right), incluíndo nunha soa tarxeta a preamplificación e a dixitalización.*

A DBO [56] é a tarxeta activa con 4 canais de amplificación e dixitalización en 4.5×5=22.5 cm^2, incluíndo unha soa etapa de amplificación cun factor de gaño G∼40 implementada co Philips BGM1013 (35.5 dB de gaño e unha anchura de banda de 1-2 GHz). O amplificador ten unha impedancia de 50 Ω á entrada e á saída. A saída LVDS dixital permite a medida temporal e da carga a través do flanco de subida do sinal e da anchura da mesma, respectivamente. Este método de medida da carga, proporcional á anchura do sinal dixital, cóñecese como 'Charge to Width' (QtoW). Ademáis, a DBO proporciona un sinal de trigger a través da suma analóxica dos catro canais de cada DBO. A Fig. D.3 amosa unha foto da versión definitiva da DBO, chamada STEP6, xunto coa primeira adaptación feita da electrónica de referencia deseñada polo LIP en Coimbra.

A MBO [89] é a tarxeta pasiva con 32 canais, aloxando ata un máximo de 8 DBOs en 40×6=240cm^2. A MBO suministra ás DBOs a voltaxe de alimentación, os niveis de umbral (*threshold*) suministrados vía DACs, os sinais de test e as pistas para tódolos canais e o sinal de trigger. A nivel da MBO, ó sinal de trigger de cada DBO é sumado outra vez para obter un único sinal por cada MBO.

A electrónica de preamplificación e dixitalización é alimentada por unha tarxeta de baixa tensión [108], deseñada por A. Gil do IFIC, baseada en módulos de conversión DC-DC tendo en conta o consumo de 0.5 W/canle da electrónica. Dúas de estas tarxetas son necesarias para alimentar cada un dos seis sectores de RPC do muro de HADES, e están preparadas para monitorizar a voltaxe e a corrente.

Por último, o sistema de adquisición baséase nunha tarxeta TDC Readout Board (TRB) [86] deseñada no GSI. A TRB implementa 4×32 canais de HPTDC, deseñado no CERN e que se caracteriza por unha resolución temporal de σ_T=40 ps/canle. O sinal de trigger suministrado por cada canle das DBOs é necesario para a tarxeta de adquisición.

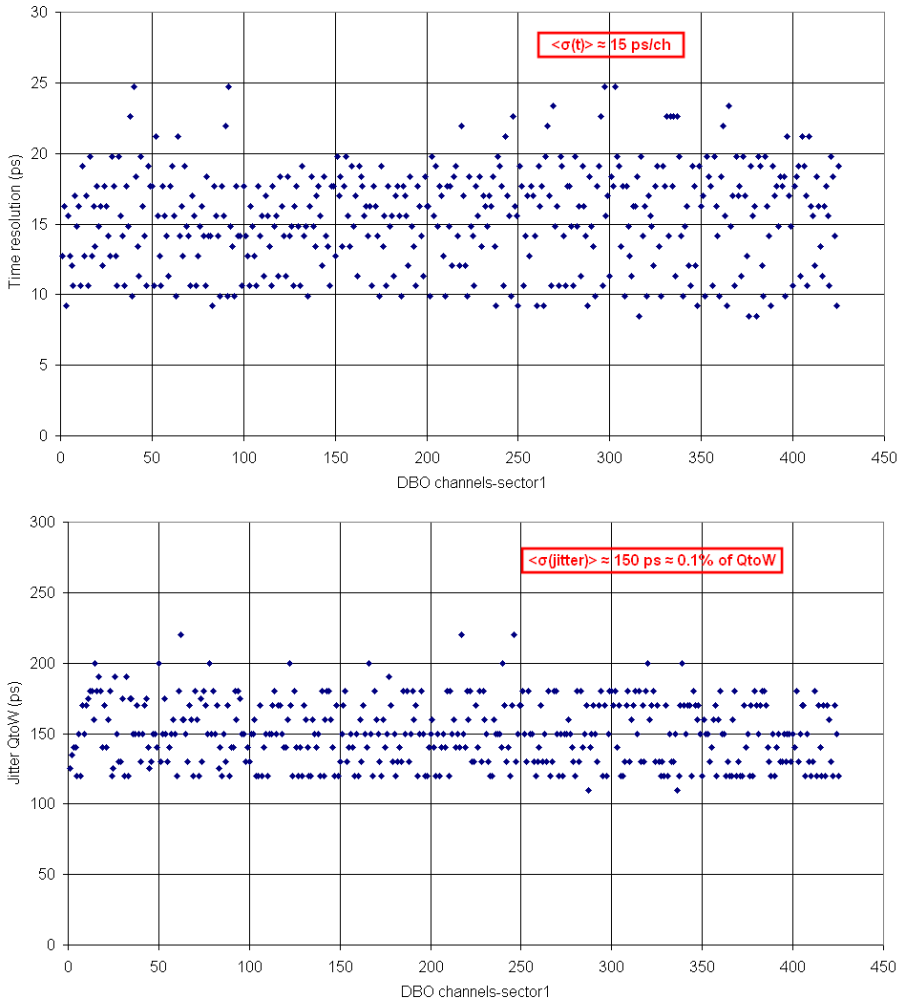


Figure C.4: *Medidas da electrónica final correspondente a un sector completo. Arriba: resolución temporal por canle. Abaixo: fluctuación (jitter) na medida da carga a través do algoritmo QtoW.*

C.3 Resultados da electrónica

A continuación, amosaranse unha serie de resultados, tanto sobre a electrónica como sobre o conxunto da electrónica, RPC e TRB. Os máis relevantes son medidas da resolución temporal da FEE e do sistema completo coa RPC, e medidas da carga co algoritmo QtoW.

A Fig. D.4 amosa os resultados propios da electrónica, incluíndo a DBO e a MBO, como resposta ó sinal de test. A figura superior presenta a resolución temporal dos canais individuais da versión final de electrónica usada na montaxe do primeiro sector RPC na posta a punto do experimento. O valor medio da resolución temporal por canle obtido é σ_T=15.4 ps. O valor medio para os canais correspondentes ós seis sectores é σ_T=16.4±5 ps/canle. A figura inferior presenta o *jitter* no flanco de

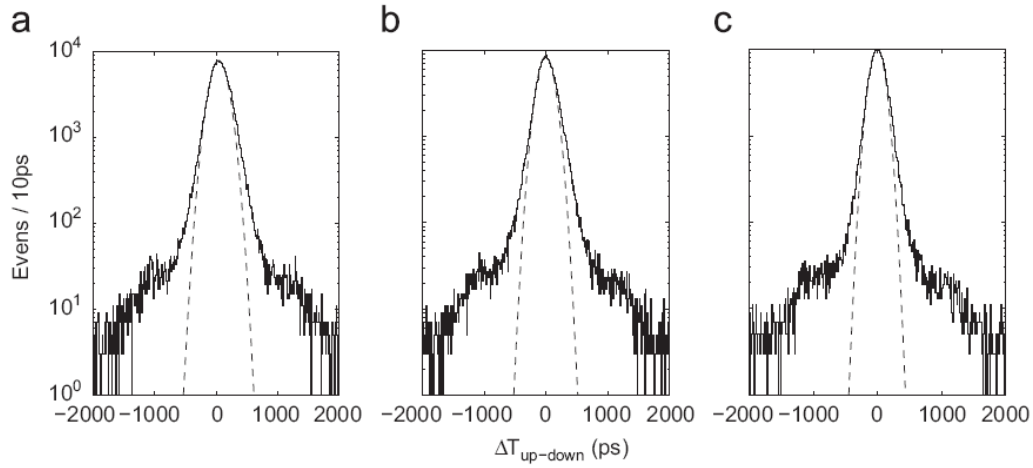


Figure C.5: *Distribucións de $\Delta t_{up-down}$: (a) sen correccións (σ_T=135/$\sqrt{2}$=96 ps, colas en 3σ do 2.5%); (b) despois da corrección en posición (σ_T=122/$\sqrt{2}$=86 ps, colas en 3σ do 2.5%); e (c) despois da corrección en carga para o sector completo (σ_T=103/$\sqrt{2}$=73 ps, colas en 3σ do 2.2%).*

baixada do sinal LVDS, que é unha medida da resolución do algoritmo QtoW. O valor medio obtido é Δt_{QtoW}=150 ps, e tendo en conta que a resposta ó sinal de test ten unha anchura media de w_{ch}=200±10 ns, corresponde a un 0.1% do valor total.

Os resultados pertencentes ó conxunto da RPC, a electrónica e o TRB amósanse nas Figuras D.5 e D.6. A Fig. D.5 presenta a resolución temporal do detector completo nun feixe (*beam*) de C a 2 AGeV con brancos de Nb e Be, medida a partir do axuste gaussiano da diferencia de tempos entre dúas celdas superpostas. O valor obtido sen correccións é σ_T=96 ps/canle, con colas en 3σ do 2.5%. Unha vez aplicada a corrección en posición, a resolución temporal mellora ata un valor de σ_T=86 ps/canle, mantendo as colas en 3σ. Por último, aplicando tamén as corrección en carga, a resolución temporal mellora aínda máis ata unha σ_T=73 ps/canle, mellorando as colas en 3σ ata o 2.2%. A superposición parcial das dúas capas no deseño dos sectores de RPCs elimina completamente as colas longas no tempo para unha fracción grande de eventos [75].

A Fig. D.6 mostra o espectro de carga medido a través do algoritmo 'Charge to Width' (QtoW) dun lado dunha celda RPC, medido nun experimento con raios cósmicos. Non está en unidades de carga, senón en bins do TDC. Podemos diferenciar, claramente, dúas rexións:

1. Avalanchas normais e pequenas, correspondentes á rexión do primeiro pico (TDC bins<2000.)

2. *Streamers* ou sinais de gran carga, correspondentes a zoa abombada despois do pico (2000<TDC bins<8000).

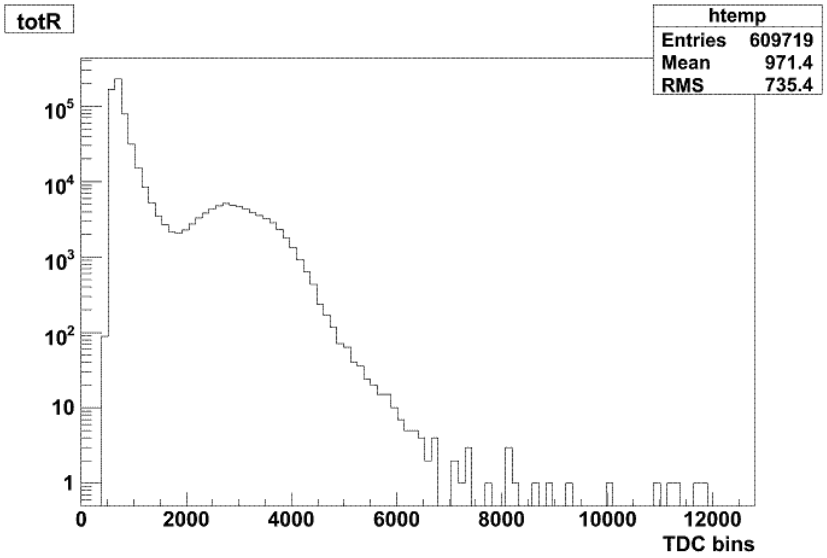


Figure C.6: *Espectro de carga QtoW para un dos lados dunha celda, medido nun experimento de raios cósmicos.*

Tendo en conta esta última figura, o algoritmo de QtoW implementado na DBO da electrónica do detector é suficiente para percorrer todo o rango de cargas das tRPCs do espectrómetro HADES, diferenciando claramente as avalanchas normais dos *streamers*. Este é un dos requisitos máis importantes deste muro de RPCs, poder verificar rapidamente se estamos cun nivel de *streamers* normal ($\leq$10%) ou xa entramos en modo *streamer*.

De seguido, móstranse outras características interesantes da electrónica de amplificación e dixitalización deseñada para o muro de RPCs de tempo de voo do espectrómetro HADES:

- Consumo <0.5 W por canle.
- Nivel de ruido á entrada do amplificador <100 μV_{RMS}.
- Nivel de *crosstalk* por debaixo do 1%, desaparecendo para umbrales maiores de 3-4 mV.
- Resolución temporal da electrónica ó nivel de σ_T=16$\pm$5 ps/canle, aumentando ata 40$\pm$5 ps/canle se incluímos a TRB.
- O rango do algoritmo QtoW antes de entrar en saturación é <4 pC, sendo a resolución en carga <10%-σ para q_p>50 fC.
- O 'umbral físico' da electrónica é 30 fC, correspondente a $\sim$1 mV.

C.4 Conclusións

As principais aportacións deste traballo inclúense dentro do campo da electrónica rápida de amplificación e dixitalización aplicada a detectores de tempo de voo (neste caso, tRPCs, unha tecnoloxía emerxida no CERN hai apenas unha década).

A construcción dun muro de RPCs de tempo de voo para o espectrómetro HADES que se atopa no GSI, en Darmstadt, Alemaña, xa está rematada. O muro está instalado definitivamente, á espera de tomar datos en diferentes experimentos no próximo ano. Dentro deste proxecto, a electrónica deseñada durante estes anos permite obter resolucións temporais por debaixo de σ_T=80 ps por canle, que nos permite que o muro de RPCs teña boas prestacións aplicado a colisións nucleares a enerxías intermedias de 1-2 Gev/A.

Todos os resultados presentados neste traballo para a electrónica foron medidos con diferentes experimentos, ben con tests electrónicos utilizando o sinal de test, ou con raios cósmicos ou feixe. As prestacións da electrónica individualmente e xunto do detector de RPCs amosa uns resultados moi interesantes que cumpren cos requisitos do muro de tempo de voo de HADES, e que fan que esta electrónica sexa utilizable en futuros experimentos, asi coma noutros detectores baseados en RPCs, como é o caso do futuro TRASGO[2] que vai deseñar o noso grupo LabCAF da USC nos próximos anos. A idea do TRASGO é desenrolar un detector capaz de traballar por si só, implementando capacidades de reconstrucción completas nunha tarxeta de adquisición "intelixente". Este detector sería de particular interese para detectar raios cósmicos na superficie terrestre, incluíndo capacidades de identificación de partículas.

[2]TRAck reconStructinG mOdule.

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